

Commercial Advances in Strained Silicon Technology

Mayank Bulsara
Co-founder and CTO
AmberWave Systems

Outline

- **Strained Silicon Introduction**
- **Commercial Strained Silicon**
- **State of the Art Demonstrations**
- **Conclusions**

Strain in Silicon

$$\text{strain}(\varepsilon) = \frac{a_{\text{final}} - a_{\text{initial}}}{a_{\text{initial}}} = \frac{a_{\text{silicon}^*} - a_{\text{silicon}}}{a_{\text{silicon}}}$$

If $a_{\text{silicon}^*} > a_{\text{silicon}}$, silicon in tension

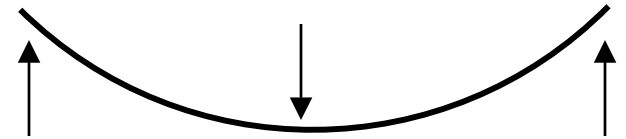
If $a_{\text{silicon}^*} < a_{\text{silicon}}$, silicon in compression

Effects of Strain

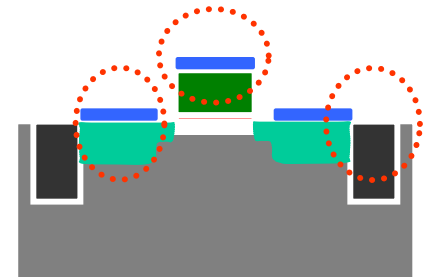
- **Lower carrier effective mass**
- **Reduced intervalley scattering**
- **Increased mobility**

How to Induce Strain in Silicon?

- Mechanical Force



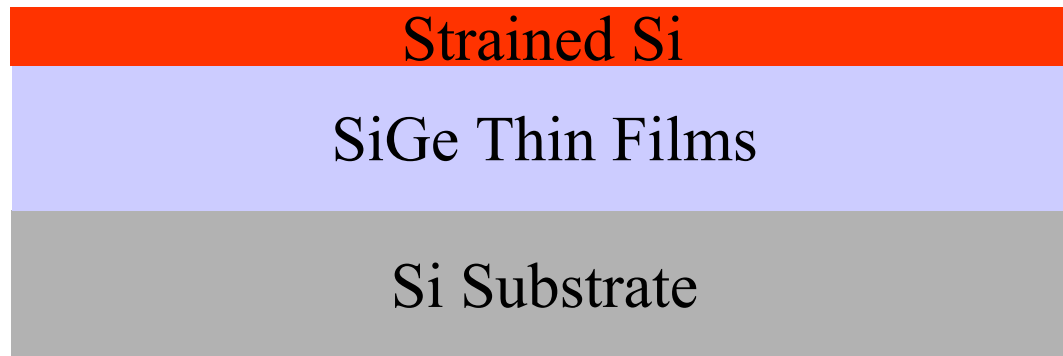
- Transistor Processing



- Epitaxial Strain-Inducing Templates

SiGe Thin Films
Bulk Si Substrate

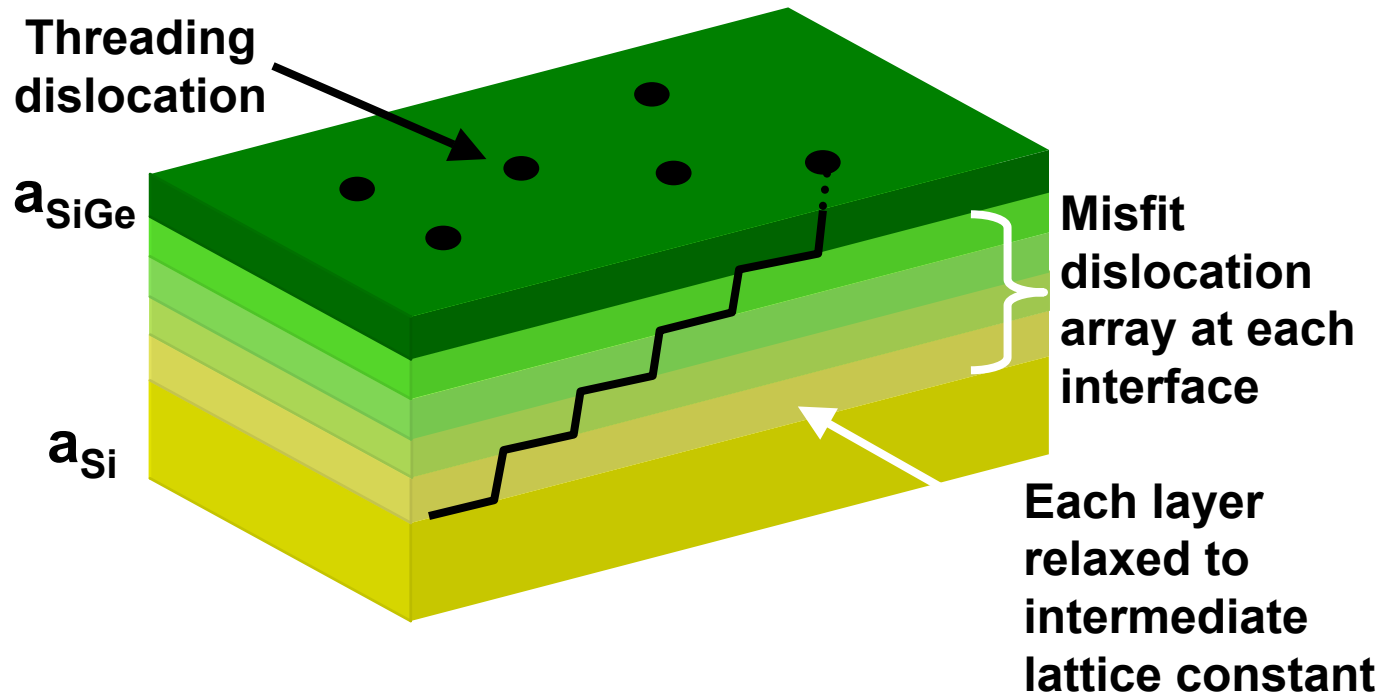
Epitaxial Strain-Inducing Templates: Most Proven Approach



$a_{\text{SiGe}} > a_{\text{Si}}$, top Si layer is stretched and placed in biaxial tension

Challenges are lattice mismatch and defect engineering

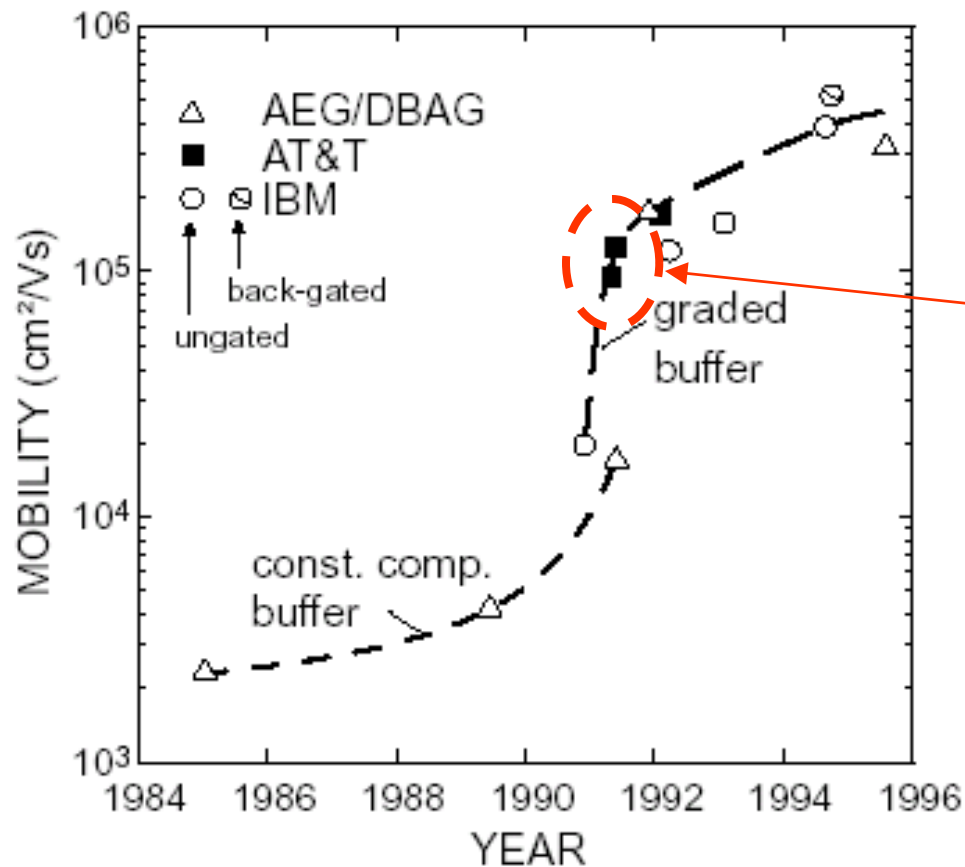
SiGe Graded Buffers



SiGe Uniform Layer TDD $\sim 10^9/cm^2$

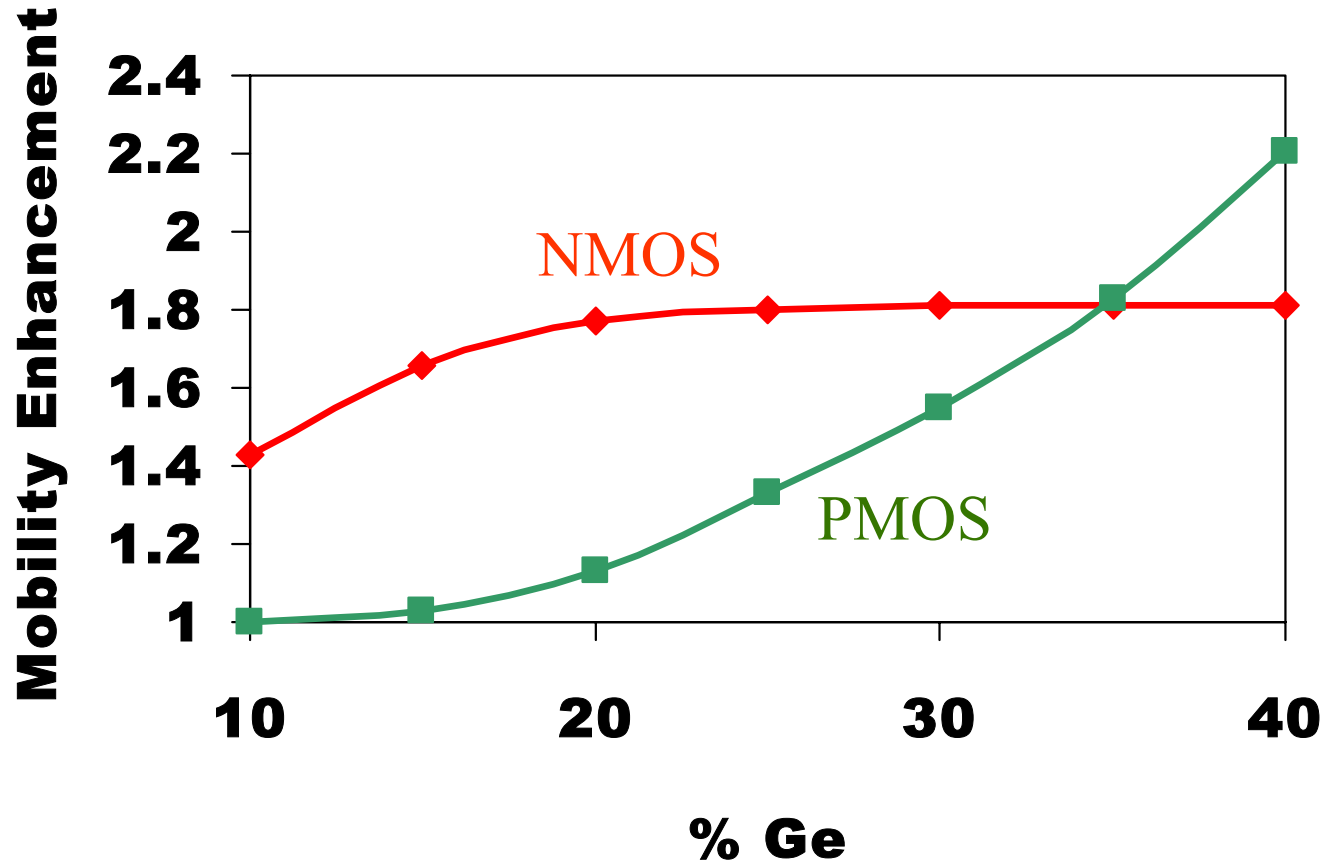
SiGe Graded Layer TDD $\sim 10^5/cm^2$ or lower

Improvement in Mobility with Graded Buffer



First
Demonstration
of SiGe Graded
Buffer in 1991

CMOS Mobility Enhancements



M.T. Currie, *et al.*, J. Vac. Sci. Technol. B, vol. 19, p. 2268 (2001)

C.W. Leitz, *et al.*, J. Appl. Phys., vol. 92, p. 3746 (2002)

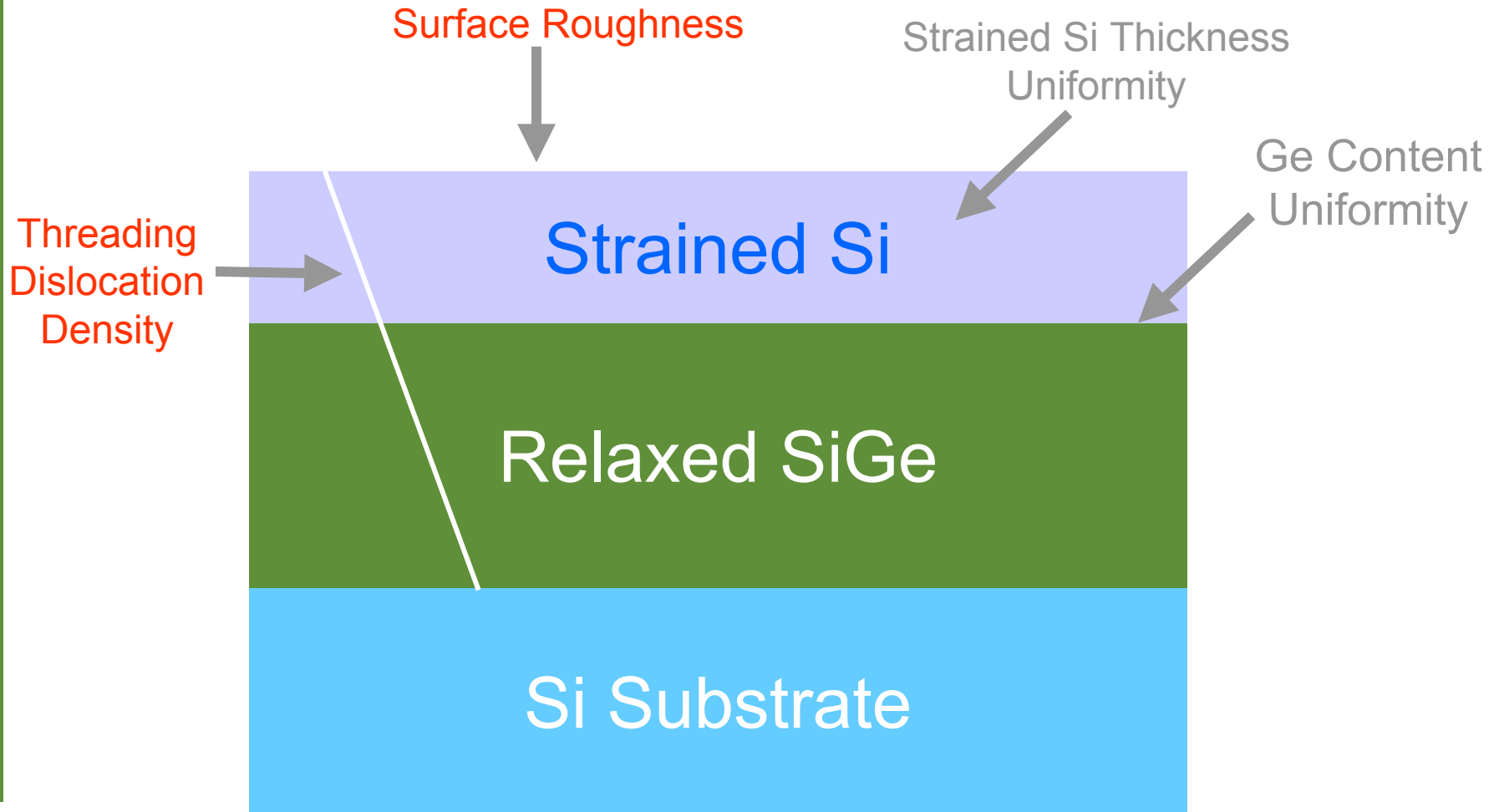
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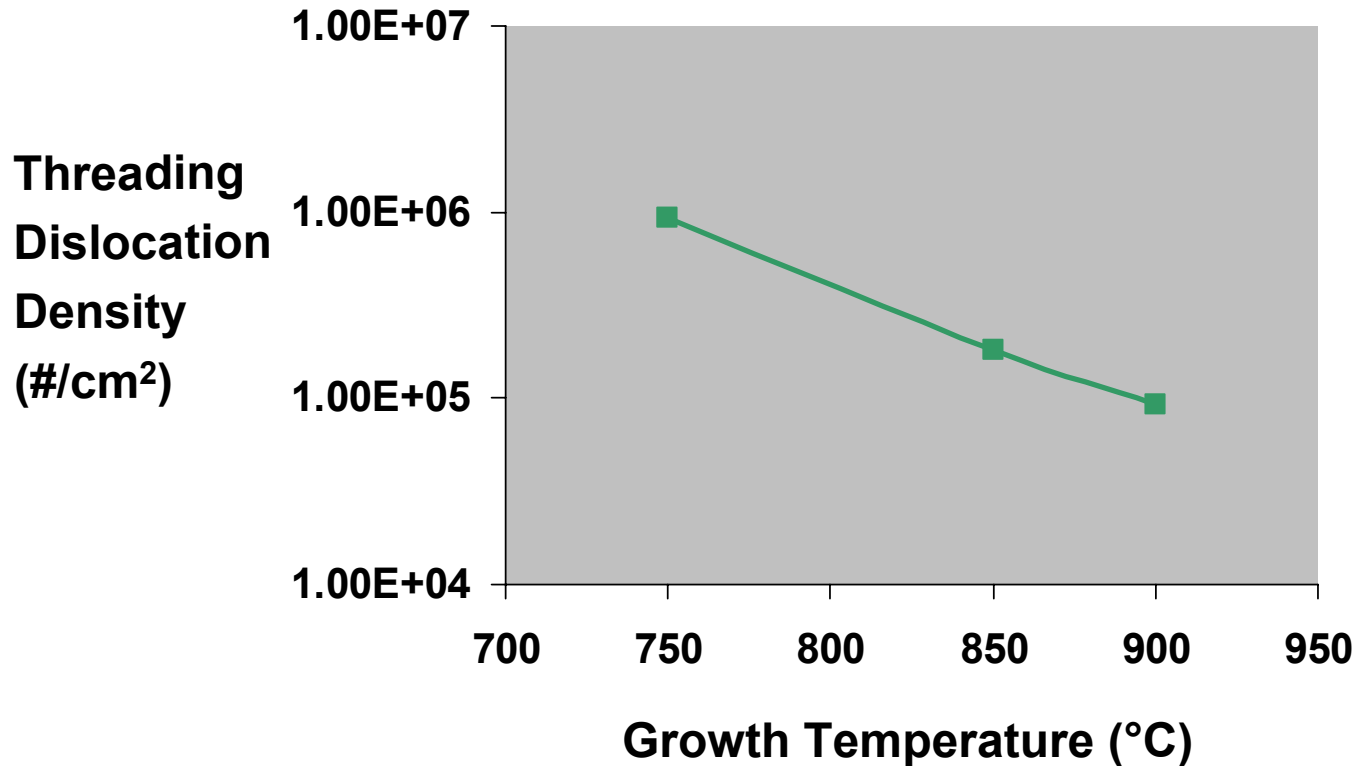
Key Strained Si Production Criteria

- **Wafer Manufacturing**
 - High quality substrates
 - Cost effective production and metrology
 - No new infrastructure required
- **Circuit Manufacturing**
 - Typical transistor engineering learning curve
 - Appropriate reliability and yield
 - No new infrastructure required

Production Strained Si-Specific Wafer Quality Metrics

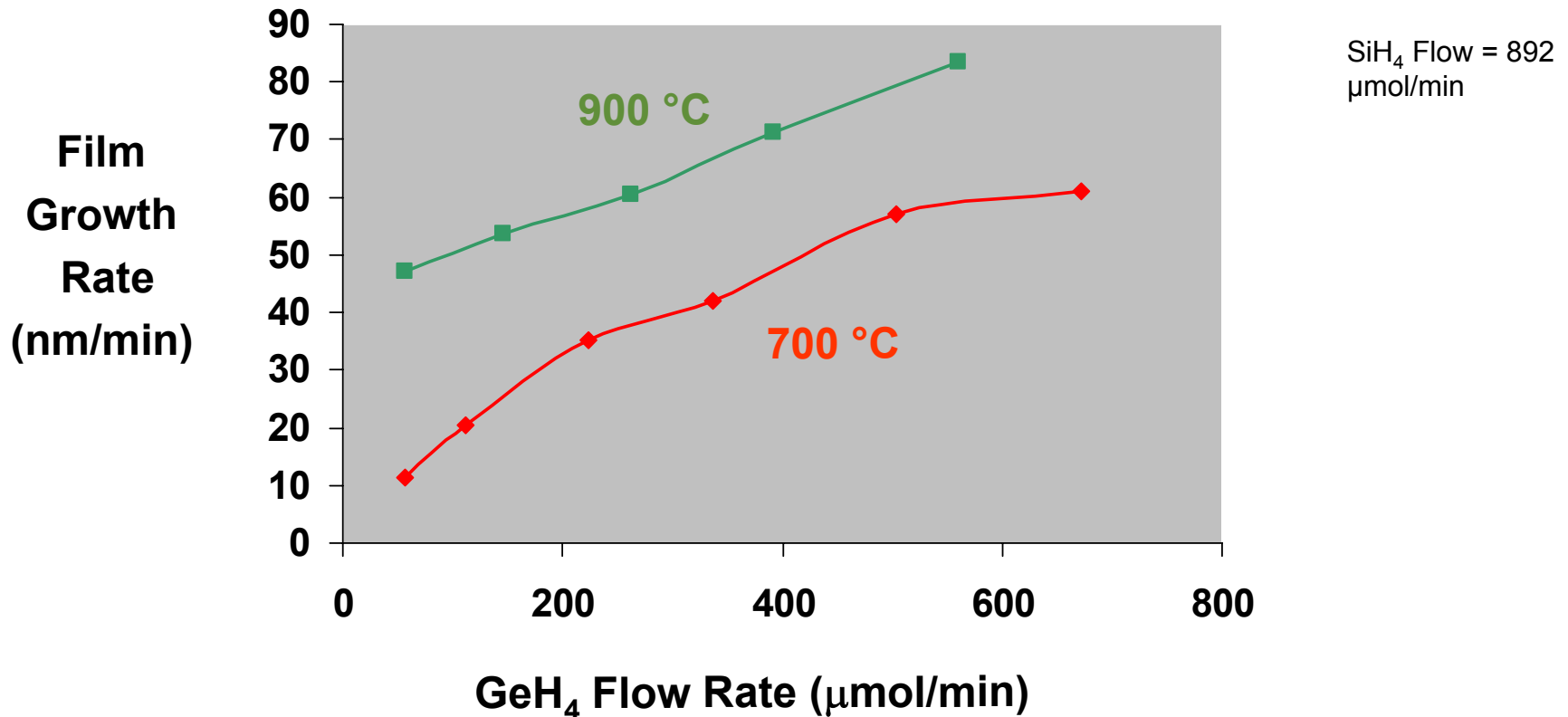


Threading Dislocation Density vs. Growth Temperature

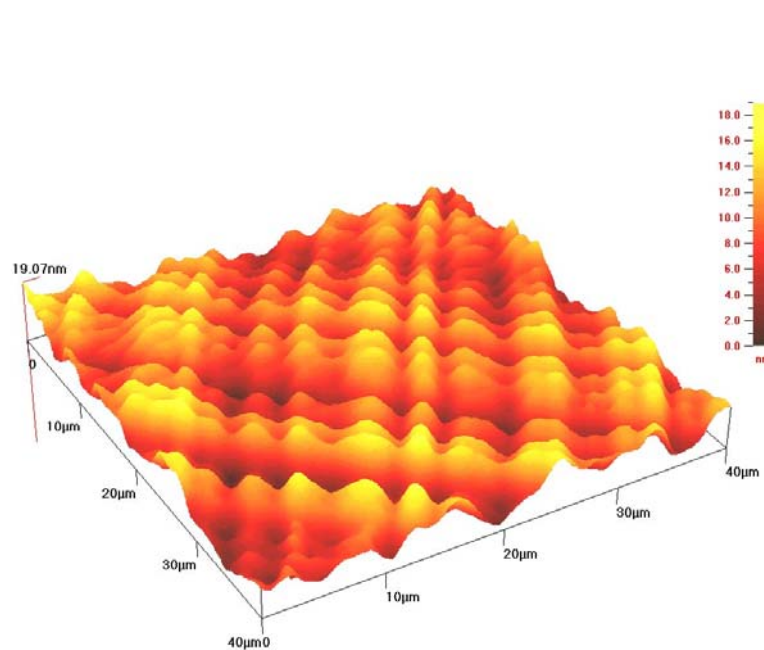


C.W. Leitz, *et al.*, J. Appl. Phys., vol. 90, p. 2730 (2001)

Growth Rate (Throughput) vs. Growth Temperature



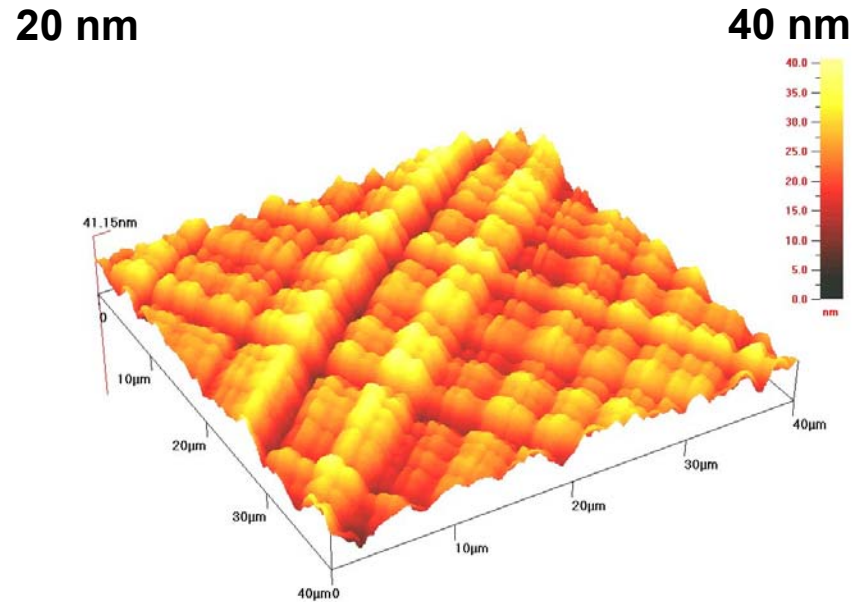
Surface Roughness vs. Growth Temperature



840 °C

RMS: 3.091 nm

Peak to Valley: 19.07 nm



900 °C

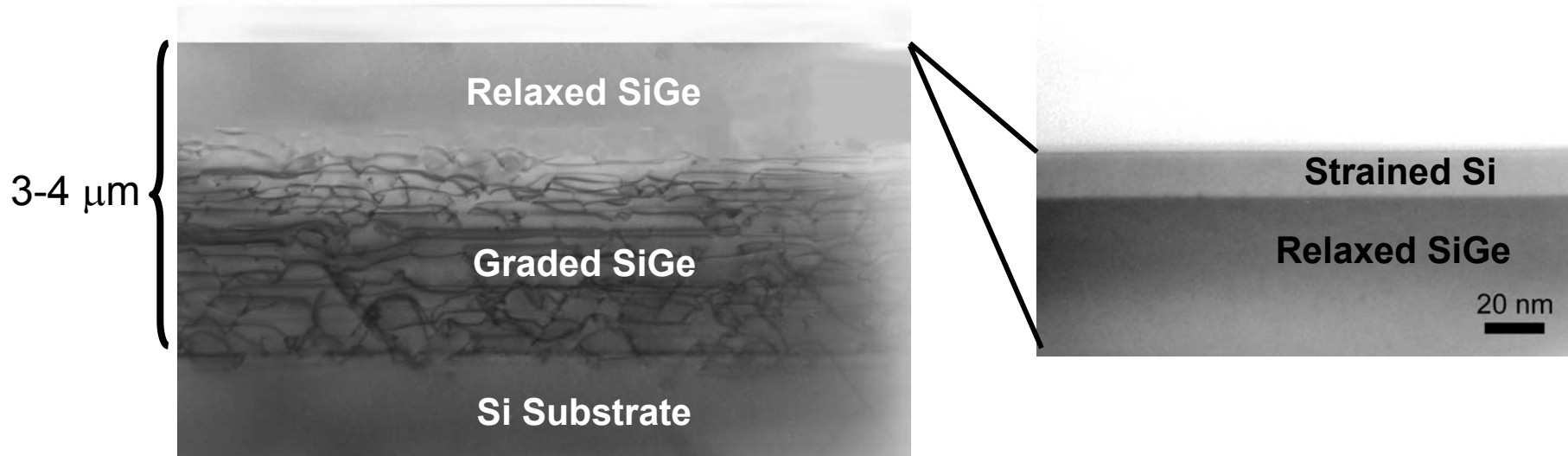
RMS: 5.670 nm

Peak to Valley: 41.15 nm

Summary of Strained Si Wafer Production Criteria

- Defect density improves at higher T
- Throughput improves at higher T
- Surface morphology degrades at higher T

Established Production Strained Si Wafer Process



Three Step Process:

1. Grow Graded SiGe Layer
2. Planarize and Polish SiGe Layer
3. Grow Device Layer with Strained Si

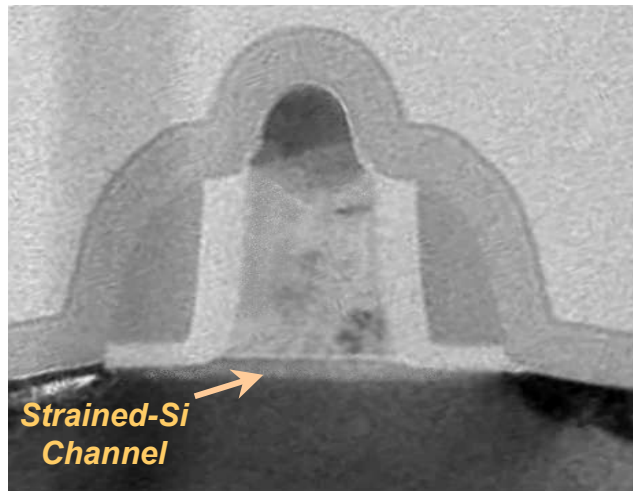
Production Strained Si Transistor Fabrication Criteria

- **Thermally stable strained Si thin films**
- **Wafer scale uniformity of strained Si properties**
- **Modifications to strained Si transistor integration schemes**
 - Minimize silicon consumption
 - Optimize thermal budget

Outline

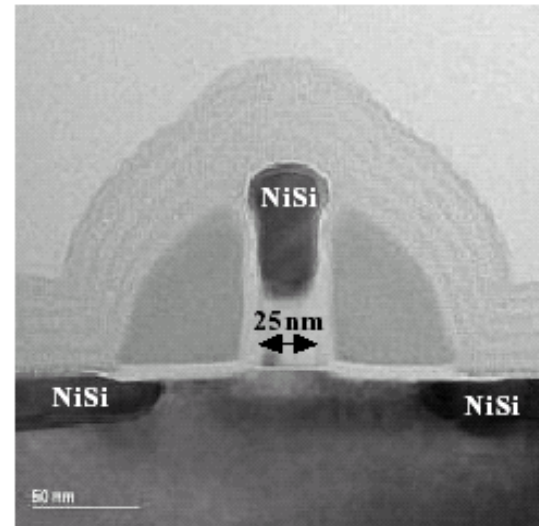
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Proven Transistor Integration for 130 and 90 nm Processes



UMC

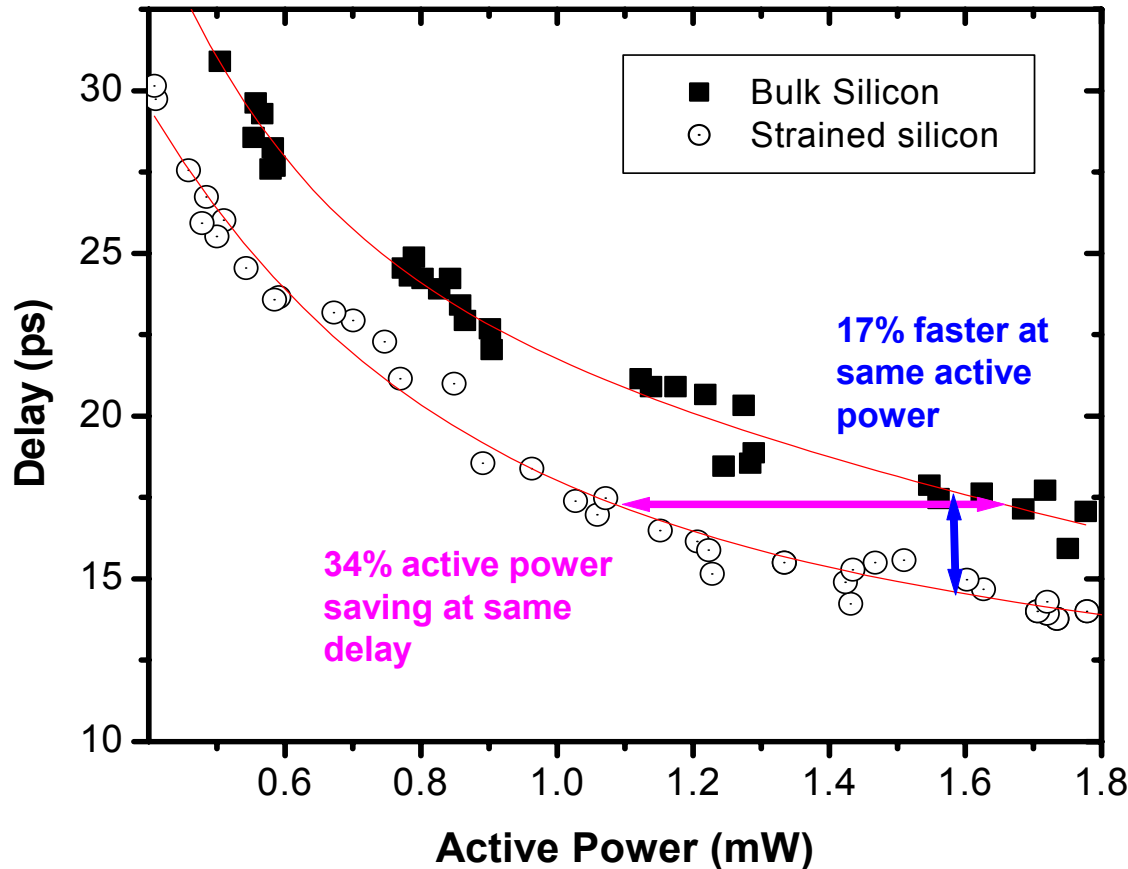
Hwang, *et al.*,
VLSI Tech. Dig., p. 108 (2003)



AMD

Goo, *et al.*, IEEE EDL,
Vol. 24, p. 351 (2003)

Strained Si Circuit Level Benefits



151 stage ring oscillators
130 nm node technology
Lg ~70nm
Vcc from 0.8V ~ 1.2V

UMC/AmberWave Systems
VLSI Technology
Symposium 2003

Strained Si Roadmap

- **1st Generation**

- 25-30% NMOS I_{dsat} improvement
- 5-10% PMOS I_{dsat} improvement

- **Future Generations**

- Substrate-based PMOS performance improvements
 - C.W. Leitz, *et al.*, Appl. Phys. Lett., vol. 79, p 4246 (2001)
- Strained Si on insulator (SSOI)
 - T. A. Langdo, *et al.*, IEEE International SOI Conference, p. 211 (2002)

Conclusions

- **Research since 1991 has prepared strained Si for mainstream CMOS applications**
- **Strained Si production metrics are being addressed**
- **Proven circuit-level enhancement demonstrates the benefits of strained Si technology**