

Defect reduction of selective Ge epitaxy in trenches on Si(001) substrates using aspect ratio trapping

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Defect-free germanium has been demonstrated in SiO₂ trenches on silicon via Aspect Ratio Trapping, whereby defects arising from lattice mismatch are trapped by laterally confining sidewalls. Results were achieved through a combination of conventional photolithography, reactive ion etching of SiO₂, and selective growth of Ge as thin as 450 nm. Full trapping of dislocations originating at the Ge/Si interface has been demonstrated for trenches up to 400 nm wide without the additional formation of defects at the sidewalls. This approach shows great promise for the integration of Ge and/or III-V materials, sufficiently large for key device applications, onto silicon substrates. © 2007 American Institute of Physics. [DOI: 10.1063/1.2435603]

Ge heteroepitaxy on Si is a promising both for high performance Ge *p*-channel metal-oxide-semiconductor (MOS) transistors^{1,2} and as a potential path for integrating optoelectronic devices with Si MOS technology.³ Unfortunately, growing more than a few nanometers of Ge directly on Si leads to a dislocation density of 10⁸–10⁹ cm⁻² due to the 4.2% lattice mismatch—unacceptable for most applications. Solutions such as compositional grading^{3,4} or methods utilizing postgrowth high temperature annealing^{5,6} have been explored to alleviate this problem. However, for greater ease of integration with Si MOS a defect reduction solution involving minimal epi thickness (to minimize thermal expansion mismatch stress as well as to meet planarity requirements for Si processing) and minimal thermal budget (to allow addition of Ge at any point in the process without degrading the MOS transistor elements) may be highly desirable. Researchers have shown that these requirements may be met by selective growth of Ge in small vias (diameter ≤ 200 nm) through a dielectric mask;^{7,8} this may be explained by the “epitaxial necking” mechanism,⁹ although other effects may be important as well.^{7,9}

In this letter we show this approach, which we refer to as Aspect Ratio Trapping (ART), applied to larger areas. We demonstrate effective trapping of threading dislocations in trenches of arbitrary length. This is shown for Ge grown directly on Si via reduced pressure chemical vapor deposition. Ge layers as thin as 450 nm were deposited in SiO₂ trenches having aspect ratio (AR=trench height/width) > 1. Trenches were fabricated by conventional photolithography and reactive ion etching (RIE) techniques.

These experiments began with 200 mm diameter *p*-type Si(001) substrates, 6° off cut along the [110] direction, and a 500-nm-thick thermal oxide. The oxide layer was patterned into trenches along [1 $\bar{1}$ 0] having 0.2–2.5 μm width using a conventional photolithography and RIE. It is well known that RIE etching with CF_x chemistries can leave a fluorocarbon residue on the surface causing defective epitaxial layers in subsequent growth.¹⁰ In order to remove this in preparation for epi, an oxygen plasma ashing step (800 W at 1.2 Torr for 30 min) was carried out after RIE. The patterned substrates

were then cleaned in Pirana, SC2, and dilute HF solutions sequentially. The final trench height was 490 nm after this cleaning procedure. 450-nm-thick Ge layers, comprised of a low temperature buffer layer and a higher temperature growth layer, were grown at 400 and 600 °C, respectively, using ASM Epsilon E2000 commercial grade epitaxy reactor. The detailed conditions of the selective Ge growth are published elsewhere.¹¹ Cross-sectional and plan-view transmission electron microscopy (TEM) samples were prepared by mechanical polishing and Ar ion milling. TEM images were taken on a JEOL JEM 2100 microscope operating at 200 kV.

Figures 1(a) and 1(b) show cross-sectional TEM images of Ge layers in trenches of 200 and 400 nm widths, respectively. These structures have ARs of 2.45 and 1.23, respectively. In Fig. 1(a), it is clearly shown that the dislocations originating at the Ge/Si interface terminate at the oxide sidewall below 200 nm and that complete trapping has occurred within the first 200 nm of Ge growth. This is indicated by the dashed line and the arrow in Fig. 1(a). Furthermore, there is no evidence of either defect generation along the SiO₂ sidewall or of interactions within the trench causing defects to deflect and zigzag out of the trench. As a result, a completely defect-free region is created as the growth proceeds beyond the defect-trapping region. Here, a defect-free region of about 300 nm in thickness is shown. Similarly, for the 400 nm width structure, the defect-trapping region is about 400 nm thick, as shown in Fig. 1(b), and indicated by the dashed line. The final thickness of the defect-free region was about 100 nm.

The mechanism of ART can be further illustrated using plan-view TEM images. Figures 2(a) and 2(b) show plan-view TEM images of Ge layers in trenches of 360 and 700 nm widths. The ARs were 1.36 and 0.7, respectively. Here the TEM captures the entire thickness of the Ge-filled trenches. In Fig. 2(a), it is found that the dislocations in Ge area terminate at the oxide sidewall as indicated by (1) and (2). For AR > 1, most of the dislocations were trapped by the oxide sidewall, which is not the case with AR < 1, as shown in Fig. 2(b). For this latter case many dislocations terminate at the SiO₂ sidewall as indicated by (3)–(5), but some such as indicated by (6) terminate instead at the Ge surface.

Trapping for AR > 1 has previously been predicted based on the preferred defect geometry in the <110>{111} dia-

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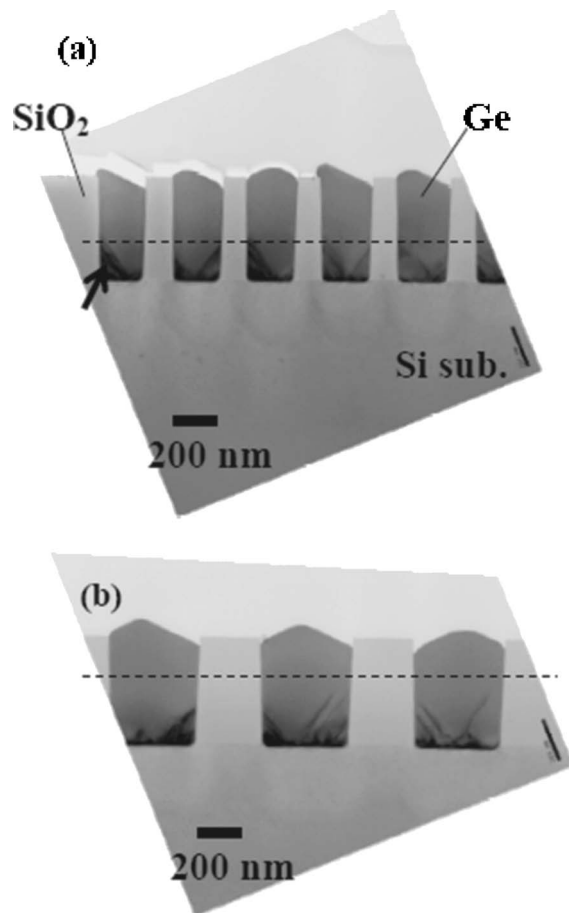


FIG. 1. Cross-sectional TEM images of Ge in trenches of (a) 200 nm (AR=2.45) width and (b) 400 nm (AR=1.23) width showing dislocations originating at the Ge/Si interface trapped by the oxide sidewall and defect-free Ge at the top of the trenches. The dashed line in each image indicates where AR is 1 (trench height is equal to its width).

mond cubic slip system.⁹ For growth on a (001) surface, misfit segments lie at the heteroepitaxial interface along the $\langle 110 \rangle$ directions, with the threading segment rising up on (111) planes in $\langle 011 \rangle$ directions, making 45° angle to the underlying Si(001) substrate as shown in Fig. 3. Thus, for $AR > 1$ threading dislocations will be trapped by a $\langle 100 \rangle$ -oriented sidewall leading to a defect-free top epilayer on Si. However, to fully understand the behavior of dislocations in small trenches, other factors may need to be taken into consideration, such as the image force exerted by the pattern sidewalls on the dislocation segment,¹² and the possible role of faceting, given the tendency of a dislocation to grow normal to the crystal growth surface.¹³

In order to definitively demonstrate regions of defect-free Ge by ART, the TEM sample shown in Fig. 2 was thinned further, removing the dislocation-trapping region and imaging the overlying defect-free region. As is typical with plan-view TEM sample preparation technique, a wedge-shaped sample is created. We used convergent beam diffraction patterns to measure the thickness at the center of the sample. This was found to be about 70 nm. Figure 4 shows the result for trench width of 290 nm; multiple adjacent trenches were completely dislocation-free except for one defect in the thickest part of the sample where the sample begins to encroach on the underlying trapping region. This is indicated by the arrow and is consistent with the cross-section TEM results, assuming the thickness of the heavily

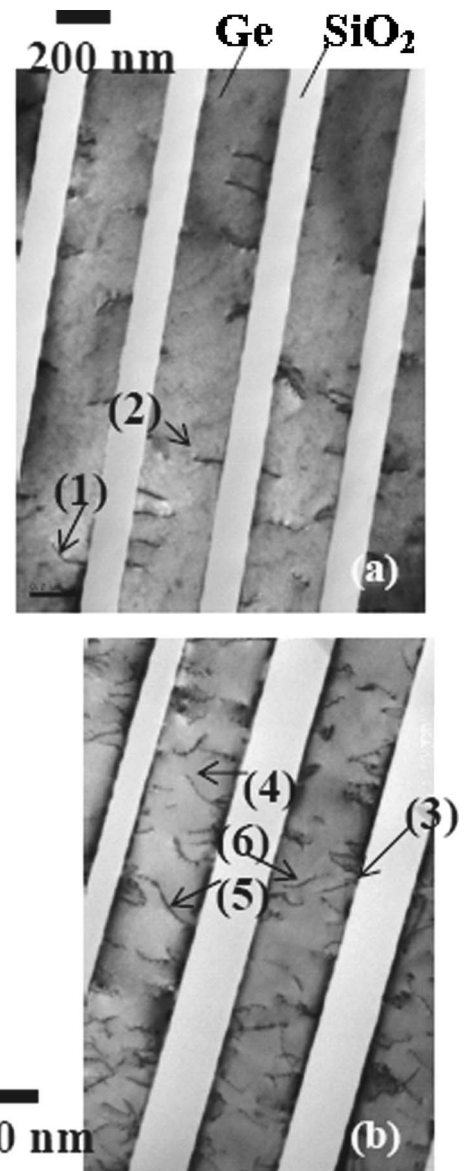


FIG. 2. Plan-view TEM images of Ge in trenches of (a) 360 nm (AR=1.36) width and (b) 700 nm (AR=0.7) width showing dislocations trapping at the sidewall at different AR.

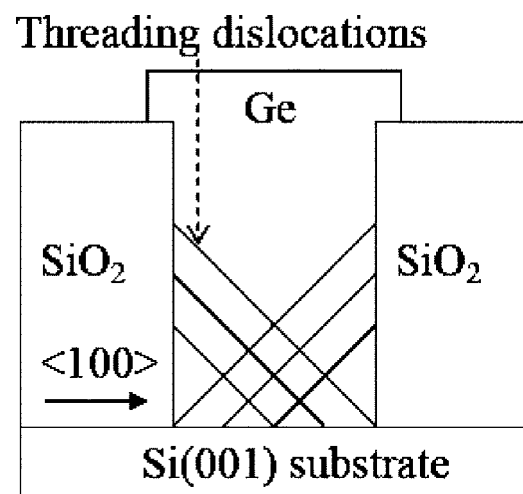


FIG. 3. Cross-sectional schematic demonstrating a possible mechanism behind ART. After Ref. 7.

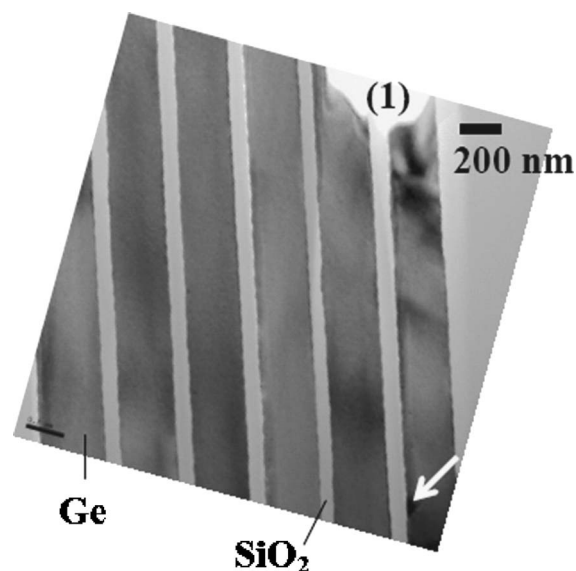


FIG. 4. Plan-view TEM image of defect-free Ge in trenches of 290 nm width without dislocation-trapping region. Note that the region at the top indicated by (1) was removed during the sample preparation and the bottom of the image as the thickest part of the sample.

dislocated region to be approximately equal to the width of the trench.

These results offer a compelling new path for adding new semiconducting materials to the Si MOS technology platform. Only conventional tools and techniques, in common use in Si complimentary metal-oxide semiconductor (CMOS) manufacturing, were used to fabricate these samples. Furthermore, the thermal budget was low enough such that the Ge could potentially be added at any time in a CMOS process. Given the growing interest in replacing Si in the CMOS channel with Ge (for p-channel MOS) and eventually with III-V materials (for n-channel MOS), it is worth noting that the feature size achieved (400 nm with full trapping) is already large enough to serve as the active area for leading-edge CMOS logic transistors, assuming, as an example, a single planarized ART region per transistor. Further

study of post-epi planarization of ART regions as well as the applicability of ART to III-V materials is required to better understand this potential.

In summary, regions of Ge up to 400 nm wide and free of near-surface defects have been demonstrated via ART in SiO₂ trenches on Si using conventional photolithography and selective growth as thin as 450 nm. All the dislocations originating at the Ge/Si interface were trapped at the oxide sidewall without the additional formation of defects at the sidewall for trenches having AR > 1. By removing the dislocation-trapping region in plan-view TEM sample preparation, defect-free Ge has been demonstrated. This approach utilized standard commercial equipment for all parts of the fabrication process and shows great promise for the integration of Ge and potentially III-V materials as well with Si MOS technology.

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