



Monolithic Integration of GaAs/InGaAs Lasers on Virtual Ge Substrates via Aspect-Ratio Trapping

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GaAs/InGaAs quantum-well lasers have been demonstrated by metallorganic chemical vapor deposition on virtual Ge substrates on Si via aspect-ratio trapping (ART) and epitaxial lateral overgrowth (ELO). Laser-structure growth is achieved in two steps: The first step is growing uncoalesced defect-free Ge stripes on a SiO₂ trench-patterned silicon substrate via ART, whereby the misfit defects originating from the Ge/Si interface are trapped by laterally confining sidewalls. Defects arising from above the SiO₂ film are reduced by using an optimized ELO process followed by chemical mechanical polishing to provide a planar Ge surface. The second step is overgrowing a GaAs/InGaAs laser structure on the virtual Ge substrate. A number of GaAs/Ge integration issues, including Ge autodoping and antiphase domain defects in GaAs, have been overcome. Despite unoptimized laser structures with high series resistance and large threshold current densities, pulsed room-temperature lasing at a wavelength of 980 nm has been demonstrated using a combination of ART and ELO. This technique is very promising for the achievement of reliable GaAs-based optoelectronic devices on Si.

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It is a well-known challenge to realize monolithic integration of high performance III-V compound semiconductors with highly developed Si-based technologies. Much effort has been made to fabricate electronic and optical devices on GaAs/Si in recent decades.¹⁻⁶ However, major problems remain unresolved, in particular, the high density of threading dislocations in GaAs layers grown directly on Si due to the 4% lattice mismatch and to the difference in thermal-expansion coefficient between the two materials. The threading dislocations act as nonradiative recombination centers in optical devices and hence lead to device performance degradation. To date, significant progress has been made in reducing GaAs dislocation density for material growth by employing various epitaxial schemes such as cycle thermal annealing,⁴ epitaxial lateral overgrowth,⁵ and growth on compositionally graded SiGe buffers.⁶ In general, while defect density decreases as epilayer thickness increases, the large thermal mismatch between GaAs and Si eventually leads to epilayer cracking and wafer warping that limit the maximum thickness of GaAs epitaxial layers on Si substrates. A crack-free III-V heteroepitaxial solution with a thin defect-filtering layer, achieved without aggressive post-epi thermally annealing steps, is highly desirable.

Ge is an ideal intermediary material between GaAs and Si because of its complete miscibility with Si and the close lattice match between bulk Ge and GaAs at room temperature.⁷ Very recently, we demonstrated low defect Ge and GaAs materials grown in SiO₂ trenches on Si via the aspect-ratio trapping (ART) method,^{8,9} where threading dislocations arising from lattice mismatch are trapped at vertical sidewalls confining the growth region. Full trapping of dislocations has been demonstrated for trenches up to 400 nm wide without the formation of additional defects at the sidewalls above 250 nm initial growth. Although the misfit dislocations are fundamentally unavoidable, they may be inconsequential to device performance if they can be trapped within a thin layer near the Ge/Si or GaAs/Si interfaces, away from the device active region. In fact, ART-based high performance Esaki diodes¹⁰ and metal-oxide-semiconductor field-effect transistor¹¹ devices using monolithically grown GaAs/Ge/Si structures have been successfully demonstrated recently. In this paper, we demonstrate 980 nm GaAs/InGaAs lasers grown on a virtual Ge substrate, for which the Ge thin film was grown on Si(001) substrates via the ART method followed by chemical mechanical polishing (CMP). The laser diodes are uncoated edge-emitting broad-area devices. Despite unoptimized laser structures have relatively high series resistance and large threshold

current densities, this ART-based approach, vis-a-vis other methods, provides a promising pathway with several unique features in achieving high performance III-V devices on Si: (i) Misfit-defect-induced threading dislocations in Ge can essentially be trapped within a limited layer thickness inside SiO₂ trenches via ART.⁸ The density of coalescence defects, which have been seen to be the major cause during coalesced growth,¹² can dramatically be reduced by enhancing epitaxy lateral overgrowth (ELO), through which large-area, low defect Ge can be obtained. (ii) GaAs overgrowth on the polished planar Ge surface enables further reduction of threading defects with buffer-layer optimization at the GaAs/Ge interface. (iii) On-axis Si(001)-based virtual Ge substrates created by the ART + ELO growth process possess off-cut surface characteristics, which lead to antiphase domain (APD) reduction in overgrown GaAs. (iv) Compatible with standard Si processing procedure based on non-off-cut Si(001) substrates. In addition, III-V/Si devices can be easily cleaved once needed.

Experimental

The substrates used in this study were 200 mm p-type on-axis Si(001). A thin SiO₂ layer was thermally grown on the Si substrate, followed by conventional photolithography and reactive ion etching techniques to form multiple sections of trenches and waffle patterns, exposing the Si surface along the [110] direction. Each section had a 0.25 μm trench width. The SiO₂ spacer between neighboring trenches varied from 0.25 to 20 μm in the various trench sections, while sections were separated by 10 μm of SiO₂. After wafer preparation and before growth, the final trench height was about 480 nm.

Two-step low pressure metallorganic chemical vapor deposition (MOCVD) processes were performed in this study. First, an epitaxial Ge layer was grown on the patterned substrate under optimized growth conditions similar to that described previously.⁸ Ge growth was terminated after the Ge layer slightly coalesced in the 20 μm spacer section (later referred to as the ELO section), which corresponds to an average layer thickness of about 4 μm. Then, a CMP process was used for planarization of the Ge-SiO₂ composite structure.¹³ Before GaAs overgrowth, the polished Ge/Si substrate was cleaned with successive dips in H₂O₂ solution and 1:50 diluted HF, with deionized water rinses between steps. In the second growth step, GaAs layers were deposited in a separate MOCVD reactor at a constant low pressure (70 Torr) by using triethylgallium and arsine (AsH₃) for buffer-layer growth and trimethylgallium, trimethylaluminum, trimethylindium, and AsH₃ for upper structural-layer growth. Before buffer-layer growth, the wafer was baked at 600°C for 10 min under H₂ overpressure followed by 2 min of As coating

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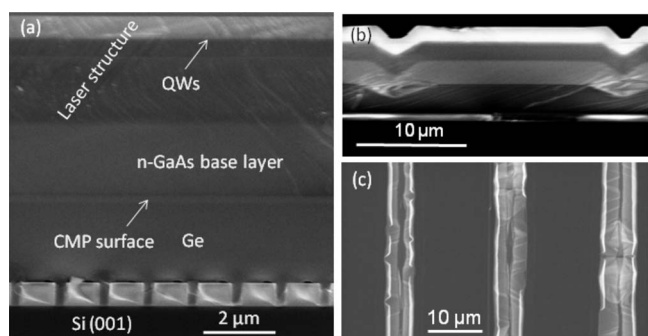


Figure 1. Cross-sectional SEM of GaAs laser structure on Ge ART virtual substrate: (a) 1 μm SiO_2 -spacer section, (b) ELO section (20 μm spacer), and (c) top-view SEM of (b).

by introducing AsH_3 overpressure. Then the growth temperature was reduced to 400°C for 30 nm GaAs buffer-layer growth followed by a three-period GaAs (10 nm)/ $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ (15 nm) superlattice structure grown at 600°C . Finally, an n-type GaAs base layer and a 980 nm GaAs/InGaAs laser structure were grown with varied growth temperatures. The laser structural growth rates were kept at 7 nm/min for the buffer layer and at 50 nm/min for the top layers. Carbon tetrabromide and SiH_3 were used for p- and n-type doping, respectively. Each growth run contained both a GaAs(001) substrate and a Ge(001) substrate, in addition to the Ge ART virtual substrate, for comparison.

Results and Discussion

The virtual Ge ART substrate was observed by optical Nomarski microscopy before GaAs overgrowth. These post-CMP wafers showed a smooth surface morphology in all sections except for the ELO trench section, in which linear depressions existed due to the incomplete coalescence of the Ge film over the oxide spacer. After GaAs overgrowth, the surface looked very smooth in the scanning electron microscope (SEM) on all sections except for the ELO section, which retained the pregrowth Ge surface feature. Cross-sectional SEM images of the laser structure are shown in Fig. 1, where Fig. 1a was taken from a trench-patterned section with 1 μm SiO_2 spacer, while Fig. 1b was taken from the ELO section. In Fig. 1c, the top-view SEM image of the ELO section indicated that the overgrown film coalesced with a variable facet, which suggests that the linear depression needs to be removed or electrically isolated for laser-device fabrication. In this study, lasers were not fabricated on the ELO section due to experimental limitations.

Room-temperature photoluminescence (PL) mapping was conducted for lasers grown on multisection virtual Ge ART substrate using a 514 nm Ar laser for optical excitation at 30 mW output power. Because the GaAs cap layer has strong absorption of the laser line, the GaAs cap layer was etched off under identical etching conditions, for all inspected samples, before PL measurements. Mapping results showed that the ELO section demonstrated the best PL characteristics of all the patterned sections, which confirmed the results obtained from etch pit density (EPD) analysis on virtual Ge ART substrates, from which the lowest EPD has been demonstrated from ELO regions.¹⁴ In Fig. 2, single PL spectrum results measured from the 1 μm spacer section and ELO section are compared to those grown on GaAs and Ge substrates. All samples were grown under the same conditions. The figure shows that the PL peak intensity measured from the ELO section is about 60% of that on a GaAs substrate, but is three times higher than that on the 1 μm spacer section as well as about five times higher than that on a Ge(001) substrate. This implies that the material quality varies depending on the initial ART mask pattern with which the Ge layer was grown. Although the uncoalesced ELO section demonstrated the best epitaxial quality by PL, the laser diodes were fabricated and tested from

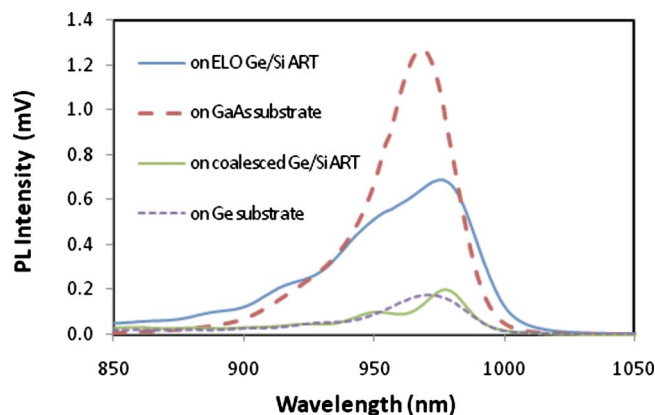


Figure 2. (Color online) Room-temperature PL spectra of GRIN SCH laser structure on various substrates (ELO section of Ge ART virtual substrate, GaAs substrate, 1 μm SiO_2 -spacer section of Ge ART virtual substrate, and Ge substrate). Samples were grown in the same growth run, and the GaAs cap layers were etched off under identical conditions to allow PL measurement.

the fully coalesced 1 μm spacer section because its planar surface allowed a more straightforward laser-device fabrication.

The key step for achieving high performance lasers on a Ge substrate is the growth of a low defect GaAs transitional base layer, which is designed as a lateral n-type conduction layer for laser diodes. It is well known that without deliberate growth optimization, issues related to APD and Ge contamination in GaAs may severely degrade or even destroy the overgrown device performance.¹⁵⁻¹⁹

In this case, because the Ge film was grown on exact (001)-oriented Si substrates, APDs become a primary concern due to the well-recognized polarity mismatch (polar/nonpolar) at the GaAs/Ge interface. Fortunately, growth calibration revealed that the tendency of APD formation on a virtual Ge ART substrate surface is different from that observed on a Ge(001) substrate. We found that APDs can be effectively avoided using an optimized GaAs/AlGaAs superlattice structure for growing GaAs on virtual Ge ART substrates. As seen in Fig. 3a, the commonly seen high density antiphase disordered networks appeared as expected in the 2 μm GaAs base layer grown on an on-axis Ge(001) substrate. However, the same base layer grown on the virtual Ge ART substrate is nearly free of APDs, as shown in Fig. 3b. We attribute this APD reduction to the crystallographic growth behavior of the Ge grown on Si via ART, which is discussed separately.²⁰ In fact, additional investigation into overgrowth on the virtual Ge ART substrate indicated that the density of APDs in GaAs layers decreases as the thickness of the polished Ge decreases. In other words, a thinner planarized Ge layer over the SiO_2 spacer leads to higher GaAs quality, which is also a desirable aspect in improving heat transfer of overgrown devices on Si. Further experimental investigations are currently underway.

Ge autodoping has long been recognized as a potential problem for growing GaAs films on Ge substrates.^{18,19} In this work, the optimal Ge growth temperature is 600°C , which is lower than the GaAs-based laser diode growth temperature ($\sim 680^\circ\text{C}$). To avoid Ge film decomposition and possible contamination to the growth environment, the GaAs base layer is grown at 600, 630, and 680°C after growing the GaAs/AlGaAs superlattice at 600°C . During the base layer growth, the Si doping level is deliberately increased at each temperature step to the maximum value that yields good surface morphology at that temperature. This incremental increase of growth temperature and Si doping has been proven to successfully suppress Ge vapor-phase contamination and maintain superior base-layer surface morphology. The laser structure and quantum-well structures were grown on top of this base layer. In Fig. 4, secondary-ion mass spectrometry (SIMS) shows the epitaxial layer and doping

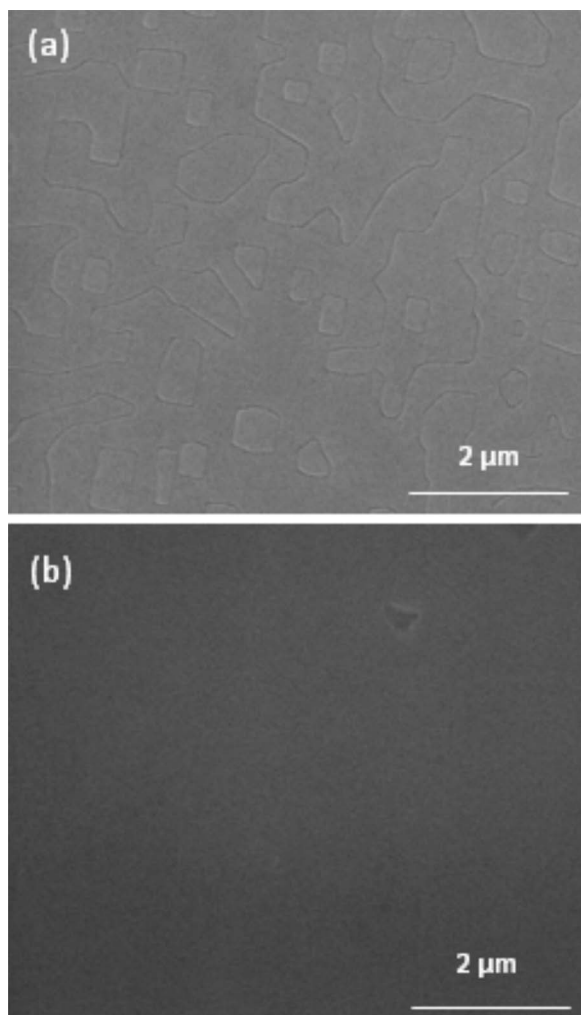


Figure 3. Top-view SEM image of 2 μm n-GaAs base layers grown under the same conditions (a) on exact Ge(001) substrate and (b) on virtual Ge ART substrate from 1 μm SiO_2 -spacer section. Significant reduction of APDs is evident for the virtual Ge ART substrate.

profiles of the simple graded index separate confinement heterostructure (GRINSCH) laser structure. Ge background doping was controlled below the detectable level in the laser structure, and its negative influence on laser performance can be neglected.

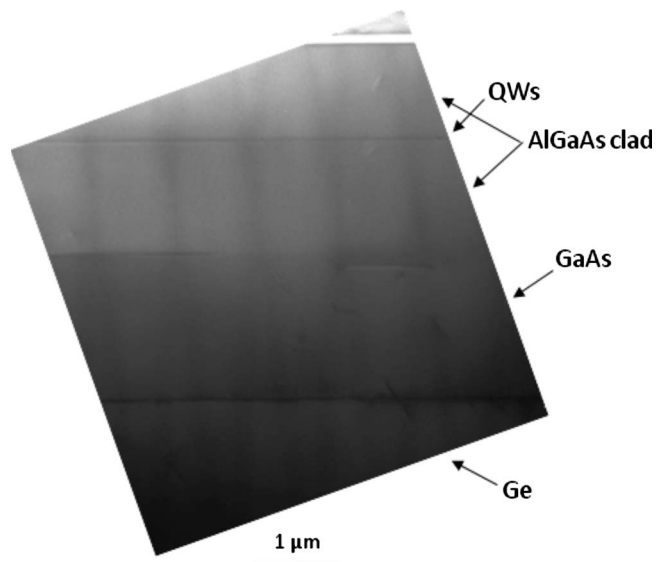


Figure 5. Cross-sectional TEM image of GRINSCH laser structure grown on a virtual Ge ART substrate.

Transmission electron microscopy (TEM) was used to characterize the defect structure of the laser material on Si. A cross-sectional TEM image of the area is shown in Fig. 5. For optimized Ge/Si growth, very few stacking faults or microtwins were observed near the boundary of the SiO_2 mask, although voids were observed in the Ge layer at the coalesced region above SiO_2 surfaces. The EPD result of the coalesced Ge layer in similarly patterned sections (1 μm spacer) is in the mid 10^7 cm^{-2} after CMP. In this work, the defect density of the active layer of the laser structure is believed to be in the level of low 10^6 cm^{-2} or high 10^5 cm^{-2} , because the optimized overgrowth steps, such as buffer layer, superlattice structure, and step-ramped temperature process, result in further defect annihilation and redirection at the GaAs/Ge interface.

The lasers grown for these experiments were simple gain guided broad-area edge-emitting structures fabricated from the 1 μm spacer section. The schematic cross-sectional laser-stripe geometry is shown in Fig. 6. Laser stripes of 20 μm were formed along the [110] direction by wet etching into the p-cladding layer. n-Contact channels of 20 μm width were formed by further wet etching into the n-GaAs base layer, evaporating Ni/Ge/Au/Ni/Au contacts and annealing. The distance from the edge of the contact to the edge of

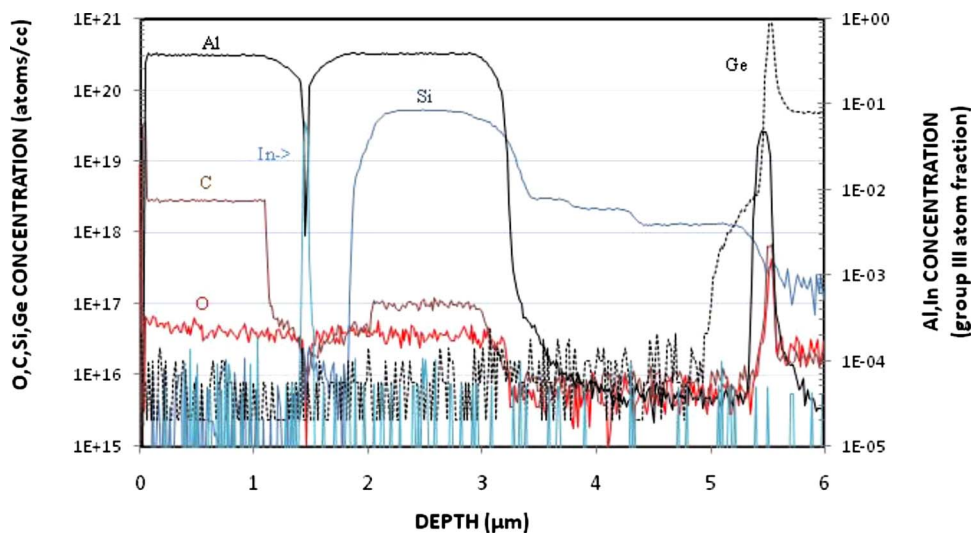


Figure 4. (Color online) SIMS profiles of Al, C, O, Si, and Ge for GRINSCH laser structure grown on a virtual Ge ART substrate. Ge diffusion from the substrate is effectively blocked by the superlattice layer and GaAs base layer.

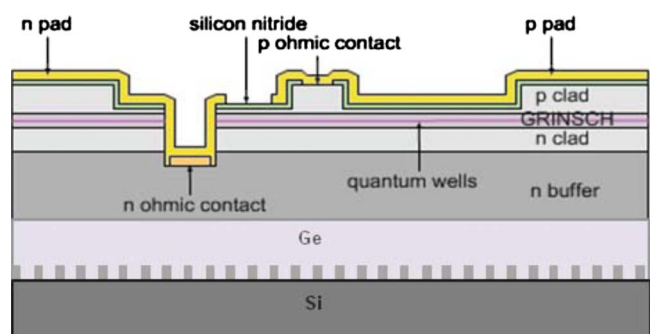


Figure 6. (Color online) Schematic cross section of processed laser structure geometry using Ge ART virtual substrate.

the ridge is 10 μm . A 200 nm thick nitride was used as the electrical isolation layer. Ti/Pt/Au was evaporated for the p-ohmic contact as well as the probe contact pads. After lapping the substrates to about 100 μm thickness, laser bars were cleaved, forming laser facets along the $[1\bar{1}0]$ direction. The cavity length of the tested laser diodes is 390 μm in this study.

To quickly and effectively analyze the quality of the laser material grown on virtual Ge ART substrates, lasers diodes were simply probe tested on unmounted bars under pulsed conditions at room temperature (with 1 μs current pulses at a repetition rate of 1000 Hz). Although this pulsed laser operation would have relatively high resistance and high threshold currents, it quickly provided direct information of the first trial laser material quality for the integrated devices based on ART.

Figure 7 shows the room-temperature current–voltage and light output power vs forward-injection current characteristics. The forward laser turn-on is about 1.5 V and the threshold current is about 240 mA, corresponding to a threshold current density of 3 kA/cm^2 .

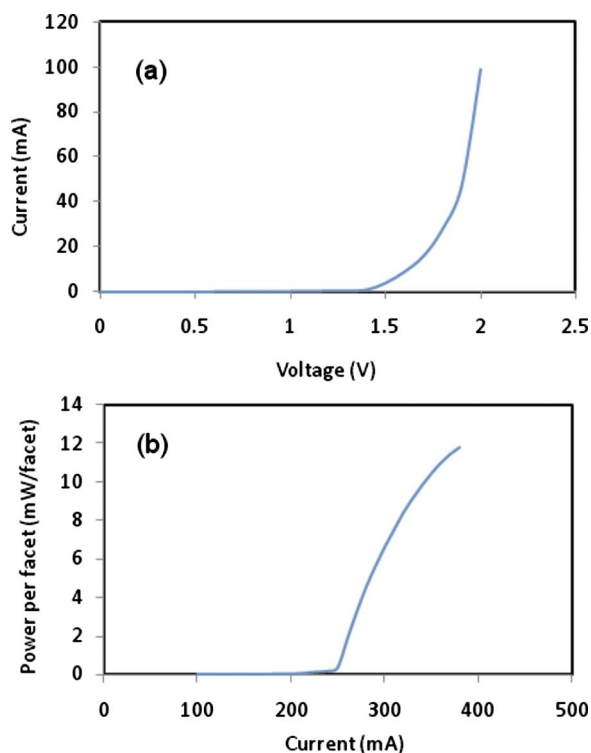


Figure 7. (Color online) Uncoated laser stripe characteristics of (a) laser current vs voltage and (b) light output power vs laser current. The maximum driving current is 380 mA.

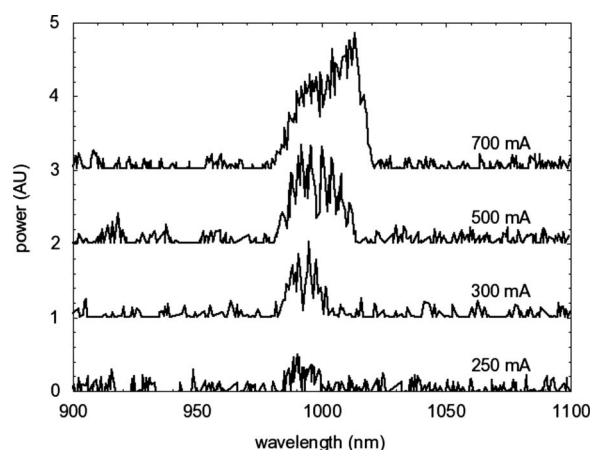


Figure 8. Laser spectrum emission measured under driving currents of 250, 300, 500, and 700 mA.

These values are comparable to that of reported results.^{6,21-23} Without facet coating, peak power as high as 12 mW per facet and a differential quantum efficiency of 22% were obtained.

As seen in Fig. 7b, the gradual decrease of the differential quantum efficiency with the increase of drive current is an indication of device self-heating phenomena related to poor heat dissipation. In our simple test configuration, heat accumulated because the laser was pressed against the chuck only by the pressure applied by the test probes. Because SiO_2 has poorer thermal conductivity than Ge and Si, the SiO_2 ART mask also retarded the heat transfer from the device to the Si substrate. Standard device-down solder bonding would eliminate both of these thermal barriers.

The laser spectrum, as shown in Fig. 8, is typical of multiple longitudinal and spatial-mode oscillation. The peak wavelength of the lasing spectrum was close to 988 nm at 300 mA drive current and moved closer to 1013 nm at 700 mA. This peak wavelength redshift is believed to be caused primarily by the device self-heating as mentioned above.

Conclusion

GaAs/InGaAs quantum well lasers of 980 nm have been demonstrated by MOCVD on virtual Ge ART substrates. Broad-area, edge-emitting devices showed promising performance characteristics under pulsed operation modes, indicating that high quality GaAs-based materials can be achieved via ART using Ge as an intermediate transition layer. Ge material quality, layer thickness, and the initial GaAs growth are the key variables for achieving high performance lasers on Si. Superior epitaxial quality of the initial Ge layer grown in the ELO section has been confirmed by PL characterization on overgrown laser structures. A GaAs/AlGaAs superlattice structure and step-ramped n-GaAs growth have been found to effectively suppress APD formation and eliminate Ge contamination in overgrown layers. It is believed that a surface favorable for APD reduction is formed after CMP for ART-based Ge growth on $\text{Si}(001)$ substrates. Also, CMP introduced an interface enabling flexible growth optimization to further reduce the threading-dislocation propagation. Although the laser structures demonstrated in this work showed relatively high threshold current density, much better device characteristics are expected for devices made entirely within a single ELO section. Nevertheless, these first-trial results demonstrate that practical heteroepitaxial integration of high performance GaAs-based optoelectronic devices on Si substrates is possible via ART with Ge as an intermediate template.

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