

Detailed Simulation Study of a Reverse Embedded-SiGe Strained-Silicon MOSFET

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Abstract—This paper presents an extensive simulation study of a MOSFET with reverse embedded-SiGe (Rev. e-SiGe), a new strained-silicon concept that utilizes elastic relaxation of a buried compressive SiGe layer to induce tensile strain in the channel. Simulations were executed to calculate the channel stress for device structures with a gate length between 32 and 10 nm, and including 4900 different combinations of the device parameters. The device parameters most critical for determining the channel stress are identified, and it is shown that optimization of the device structure to maximize the channel stress can be understood in a simple manner involving only two underlying variables, the $t_{\text{SiGe}}/t_{\text{Si}}$ ratio and the silicon/SiGe island aspect ratio. A study of the practical limits to the critical determinants of channel stress is described, and the channel stress for optimized structures within these practical limits is simulated. The Rev. e-SiGe technique is shown to be effective, inducing a level of stress comparable to or exceeding conventional strained-silicon techniques, and it is shown to be scalable down to a gate length of 10 nm. An enhanced Rev. e-SiGe process is proposed involving spacer removal and gate recrystallization; simulations show that the enhanced process can nearly double the channel stress.

Index Terms—Reverse embedded-SiGe (Rev. e-SiGe), SiGe, strain balance, strained-silicon.

I. INTRODUCTION

STRAIN engineering has become a critical tool for enhancing the performance of sub-100-nm MOSFETs, and a great variety of strain techniques have been developed [1]–[11]. However, each of these techniques has limitations; for example, the magnitude of strain is often not as large as desired, and for many of the techniques the channel strain decreases as the device is scaled down. It has proven to be especially difficult to maintain strain and strain-related current enhancement in ultrascaled NMOSFETs [7]. There is therefore a great need for novel strain techniques that induce large magnitudes of strain in the channel, that do not lose effectiveness with scaling, and that can be applied to NMOSFETs.

A new reverse embedded-SiGe (Rev. e-SiGe) strained-silicon technique was demonstrated by Donaton *et al.* in [12] that may meet these criteria. This technique uses elastic relaxation of a buried, compressively strained SiGe layer to induce tensile strain in the overlying silicon channel. The work in [12] includes demonstration of substantial drive current enhancement in sub-100-nm NMOSFETs and basic simulations of the influence of

the device parameters on the channel stress. The work in [13] and [14] also demonstrates the effectiveness of the technique in short gate length devices. These results were quite promising, and therefore, further study of this technique is warranted.

This paper presents an in-depth analysis of the Rev. e-SiGe technique for NMOSFETs in present-day and future CMOS technology nodes. Using finite-element analysis simulations, it covers the design space between $L_g = 32$ nm and $L_g = 10$ nm, the range corresponding to the International Technology Roadmap of Semiconductors (ITRS) physical gate length for the years 2005–2015 [15]. This paper has two primary goals. First, it explores the mechanisms behind the Rev. e-SiGe technique. It describes a Rev. e-SiGe fabrication process, demonstrates the mechanism by which stress is induced in the channel, shows how each of the device structural parameters influence channel stress, and demonstrates that design of the device structure to maximize channel stress can be understood simply. Second, it evaluates the effectiveness of the Rev. e-SiGe technique for present-day and future CMOS nodes. It demonstrates the magnitude of stress that a realistic, optimized Rev. e-SiGe structure can induce in the channel, and demonstrates the extent to which the stress is maintained as the gate length is scaled. It also proposes an enhanced Rev. e-SiGe technique, involving spacer removal and gate recrystallization, and shows that the enhanced technique induces significantly higher levels of channel stress. Sections II and III address the first topic, and Sections IV and V address the second.

II. Rev. e-SiGe FABRICATION PROCESS AND STRESS INDUCTION MECHANISM

A Rev. e-SiGe MOSFET fabrication process is described in Fig. 1. First, a standard CMOS fabrication process is completed through the STI step [Fig. 1(a)]. Next, the NMOSFET active areas are etched to create a small recess, and thin compressed SiGe and relaxed silicon layers are epitaxially grown on the active areas [Fig. 1(b)]. The SiGe layer is compressively strained because its lattice constant is larger than the lattice constant of silicon. Then, the process is continued through a standard gate stack process including gate oxide growth, gate and silicon nitride cap deposition, gate etch, extension, and halo implant, and spacer definition [Fig. 1(b)]. The source/drain areas are then etched [Fig. 1(c)]. This is the most important step in the process, as it creates a lateral free surface allowing the compressed buried SiGe layer to elastically expand, reducing the compressive stress in the SiGe and inducing tensile stress in the silicon above. Silicon is then regrown in the recessed source/drain areas [Fig. 1(d)] and the CMOS fabrication process is continued to completion.

The mechanism of the induction of stress in the Rev. e-SiGe structure is illustrated in the stress simulation results in Fig. 2.

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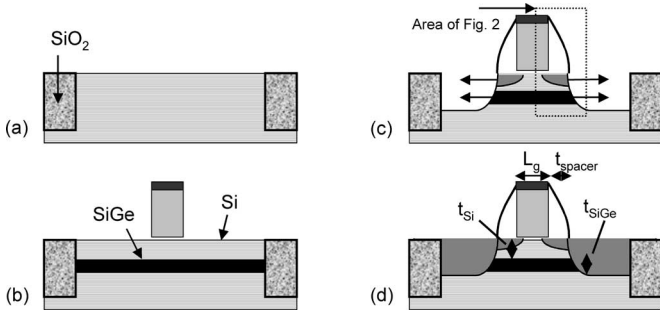


Fig. 1. Depiction of a reverse embedded SiGe MOSFET fabrication process. (a) The silicon wafer is processed through a standard STI process. (b) A thin Si/SiGe stack is grown on the STI islands, and a standard gate deposition and etch process is performed. (c) Spacers are formed and then the source/drain regions are etched. The source/drain etch step forms a lateral free surface, allowing the compressively strained SiGe layer to expand, stressing the overlying silicon layer. (d) Silicon is grown in the source/drain recesses, and the MOSFET process is finished.

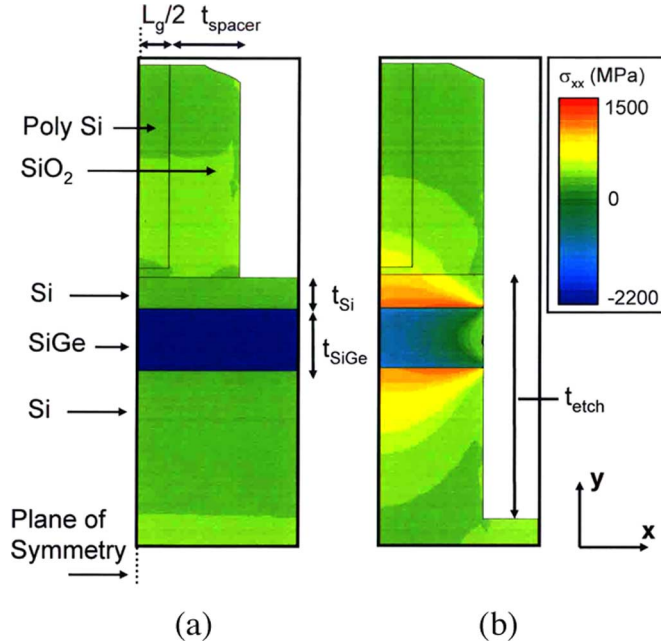


Fig. 2. Simulation of the lateral stress in the Rev. e-SiGe MOSFET structure (a) before and (b) after source/drain etch. Prior to etch, the stress in the SiGe is uniform and compressive, and there is no stress in the silicon. After etch, the compressive SiGe stress is reduced, and tensile stress is induced in the silicon above. Initial SiGe stress is -2200 MPa, $L_g = 18$ nm, $t_{\text{spacer}} = 20$ nm, $t_{\text{Si}} = 8$ nm, $t_{\text{SiGe}} = 15$ nm, and $t_{\text{etch}} = 60$ nm.

These simulations were carried out using the TSUPREM4 finite-element analysis program, which calculates the stress in a structure given an initial stress, the material elastic constants, and the fabrication process steps.

The stress profiles are shown before and after the source/drain etch in Fig. 2(a) and (b), respectively. This simulation was conducted for a device with $L_g = 18$ nm, $t_{\text{spacer}} = 20$ nm, $t_{\text{Si}} = 8$ nm, $t_{\text{SiGe}} = 15$ nm, $t_{\text{etch}} = 60$ nm, and $\sigma_{xx_SiGe} = -2200$ MPa (where σ_{xx_SiGe} is defined as the in-plane stress in the SiGe film prior to source/drain recess etch, and is equal in this case to the stress for a $\text{Si}_{0.65}\text{Ge}_{0.35}$ film on silicon). Only the right half of the device was simulated because the structure is symmetric about a vertical plane through the center of the gate. Fig. 3 shows

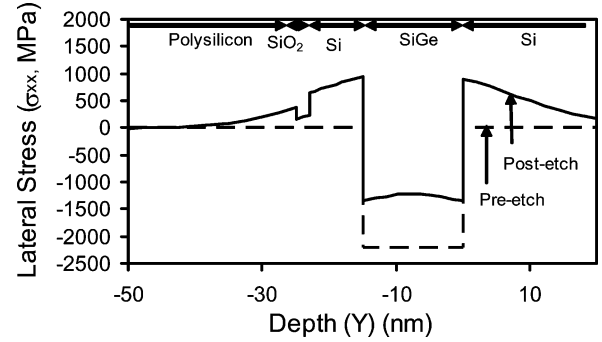


Fig. 3. Stress profile through center of gate before and after etch for structure in Fig. 2.

the horizontal stress along a vertical line through the center of the gate, both before and after the source/drain etch. As shown in both Figs. 2 and 3, prior to etch, there is no stress in the top silicon layer and there is uniform compressive stress in the SiGe layer. The etch step creates a lateral free surface, allowing the SiGe layer to expand, reducing its compressive stress and transferring tensile stress into the overlying silicon layer.

The average stress under the gate in the silicon at the gate oxide/silicon interface (called σ_{xx_SiAvg}) relative to the SiGe stress before the source/drain etch (called σ_{xx_SiGe}) is a useful figure of merit for a particular device structure. This value will be called the stress transfer efficiency (STE) in this paper, and is defined as $\text{STE} = \text{abs}(\sigma_{xx_SiAvg}/\sigma_{xx_SiGe})$. In the structure simulated earlier, the SiGe stress prior to etch is -2200 MPa, the average silicon stress after etch is 670 MPa, and the STE is 30% .

There are three important limitations to the simulations executed in this work. First, only 2-D stress simulations are considered. The 3-D effects, such as a decrease of STE in narrow-width devices, may be important but are not considered here. Second, the simulations do not account for changes to the elastic properties of materials at nanoscale dimensions. It has been shown that the elastic properties of a silicon film thinner than about 10 nm are different from its macroscopic properties [16], but consideration of nanoscale phenomena will be left for future work. Third, the anisotropic elastic nature of silicon and SiGe is ignored. The TSUPREM4 version 2001.2.0 used in this work assumes all materials are isotropic; the elastic coefficients used were for the $\langle 110 \rangle$ direction.

It is important to note that the Rev. e-SiGe device structure was actually first proposed in [17]. That work showed significant enhancement of PMOS drive current using this technique. However, it assumed that tensile stress was present in the SiGe and compressive stress was induced in the silicon, which is the opposite of what was measured in [12] and the opposite of what we have found in the simulations in this work.

III. IDENTIFICATION OF Rev. e-SiGe CRITICAL PARAMETERS AND A SIMPLE UNDERSTANDING OF STRESS MAXIMIZATION

For any strained-silicon MOSFET technology, the strain in the silicon at the gate oxide/silicon interface (the location of the inversion layer) is predominantly responsible for the enhancement of the device's drive current. For NMOSFETs with

the channel oriented in the conventional direction ($\langle 110 \rangle$ on a (001) substrate), the drive current increases with longitudinal uniaxial strain to a high level of strain beyond 1% (1700 MPa stress) [18], and therefore, the channel strain should be maximized to achieve the highest possible drive current enhancement. This section provides guidance for optimization of the Rev. e-SiGe structure to maximize the channel stress. For simplicity, this work focuses on maximizing the average lateral stress beneath the gate (σ_{xx_SiAvg}) rather than the strain. This approach ignores the effect of the vertical (y -directed) strain on the device's drive current. It also ignores the effect of the vertical stress on the lateral strain. These simplifications are reasonable because the vertical stress beneath the gate is about an order of magnitude lower than the lateral stress beneath the gate in the device structures that are analyzed.

The device parameters that determine the channel stress, are shown in the device cross section in Fig. 2. The channel stress after processing is determined by the initial SiGe stress (σ_{xx_SiGe}), the physical gate length (L_g), the spacer thickness (t_{spacer}), the silicon thickness (t_{Si}), the SiGe thickness (t_{SiGe}), and the etch depth (t_{etch}). A small number of simulations were first executed for various values of these parameters to determine which had the greatest influence on channel stress, and then, a more detailed set of simulations was executed to fully characterize the Rev. e-SiGe technique.

Three important conclusions were drawn from the first set of simulations. First, the channel stress was found to be quite sensitive to each of t_{Si} , t_{SiGe} , t_{spacer} , and L_g . Second, the channel stress was found to be insensitive to t_{etch} if t_{etch} is significantly greater than $t_{Si} + t_{SiGe}$. Therefore, the value of t_{etch} is not critical as long as it is large enough. Third, the channel stress after etching was found to be a linear function of the initial SiGe stress. This conclusion is useful because only one value of the initial SiGe stress needs to be simulated, and the channel stress can be calculated for any other initial SiGe stress using the STE: $\sigma_{xx_SiAvg} = STE * \sigma_{xx_SiGe}$.

Guided by this understanding, a large set of simulations were executed to fully characterize the Rev. e-SiGe technique. These simulations used a wide variety of t_{Si} , t_{SiGe} , t_{spacer} , and L_g , but a single value of t_{etch} and σ_{xx_SiGe} . Simulations were executed for all combinations of $t_{SiGe} = 2, 4, 8, 12, 16, 24, 32$ nm, $t_{Si} = 2, 4, 8, 12, 16, 24, 32$ nm, $t_{spacer} = 12, 14, 15, 18, 20, 22, 25, 28, 31, 35$ nm, and $L_g = 10, 13, 14, 16, 18, 20, 23, 25, 28, 32$ nm; a total of 4900 individual device design points. The t_{etch} was set to 30 nm deeper than the lower SiGe/silicon interface ($t_{etch} = t_{Si} + t_{SiGe} + 30$ nm), and σ_{xx_SiGe} was set to -2000 MPa. The STE of the structure was calculated for each design point. Practical limits to the structural variables, such as the SiGe critical thickness or limits on the silicon thickness, were ignored in these simulations.

The influence of each design parameter on the channel stress can be seen in Fig. 4. Fig. 4(a) shows the STE for different t_{Si} for a constant t_{SiGe} , and Fig. 4(b) shows the STE for different t_{SiGe} for constant t_{Si} . In these plots, the spacer thickness, t_{spacer} , is set to $1.1 \times L_g$ for each different L_g , as specified by the 2005 ITRS [13]. Fig. 4(a) shows that the STE is high for thin silicon layers, but drops greatly for thick layers. This result

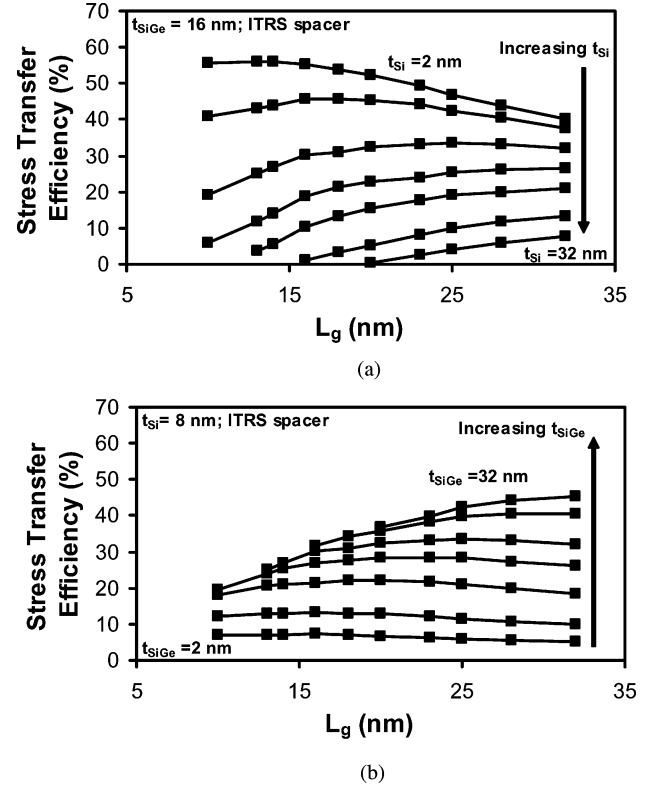


Fig. 4. STE for (a) constant t_{SiGe} and varying t_{Si} , and (b) constant t_{Si} and varying t_{SiGe} . The spacer width is equal $1.1 \times L_g$, as specified in the ITRS.

is entirely reasonable: the gate oxide/silicon surface is further from the stress-inducing SiGe layer for thicker silicon layers; therefore, the stress at this interface is lower for thicker silicon layers. The plot shows that the STE increases with decreasing L_g for thin silicon layers, but the STE decreases with decreasing L_g for thick silicon layers. The reasons for this are not obvious but are explained in detail below. Fig. 4(b) explores the effect of the buried SiGe layer thickness for a constant silicon layer thickness. For long gate lengths, the STE increases with increasing SiGe thickness, as is expected. The STE remains constant as L_g is scaled for the case of thin SiGe layers, but unexpectedly decreases with L_g for thick SiGe layers.

The decrease in the STE for short L_g is the single unexplained and undesired result shown in Fig. 4(a) and (b). This phenomenon was found to be related to the spacer thickness. In the aforementioned simulations, the spacer thickness was set to $1.1 \times L_g$ for each L_g , but this spacer thickness was found to be not optimal from a stress point of view. Fig. 5 shows the stress fields for two devices with $L_g = 10$ nm, $t_{spacer} = 12$ nm [Fig. 5(a)] and $L_g = 10$ nm, $t_{spacer} = 25$ nm [Fig. 5(b)]. A single stress contour is placed in this figure at $\sigma_{xx} = 500$ MPa and is useful for explaining why the STE decreases for small L_g . As can be seen in Fig. 5, a triangular area of low stress occurs at the edge of the gate. This low-stress area occurs because the stress is induced from the *bottom* of the top silicon layer by expansion of the SiGe layer. The SiGe is ineffective at inducing stress near the top outer edge of the silicon island. It is clear why the channel stress decreases for a small L_g ; in this case, the channel is

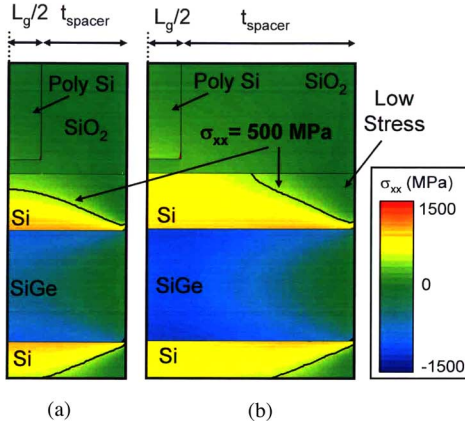


Fig. 5. Stress simulations of two structures, (a) one with a narrow spacer, $t_{\text{spacer}} = 12$ nm, and (b) one with a wide spacer, $t_{\text{spacer}} = 25$ nm. These plots show that the STE drops for the narrow spacer and short L_g because of a low-stress region that is created in the upper edge of the silicon. $L_g = 10$ nm and $\sigma_{xx, \text{SiGe}} = -2200$ MPa.

placed too close to the edge of the Si/SiGe island. To achieve a high stress level with a small gate length, a wide spacer must be used to distance the channel from the low-stress region.

The use of a wider spacer can increase the STE greatly for short gate lengths. Fig. 6 shows the results for the identical case, as in Fig. 4, except that in Fig. 6, a wider, optimum spacer was used to maximize stress transfer. The use of the optimum spacer eliminates the reduction of the STE for short L_g , making the STE nearly independent of gate length.

The discussion above shows the role of each of the variables in determining the STE: decreasing t_{Si} increases STE, increasing t_{SiGe} increases STE, and for the optimum t_{spacer} , the STE is independent of L_g . Simultaneous optimization of all of the device variables to maximize the channel stress is now considered. This requires consideration of the entire design space; the conclusions earlier came only from a limited set of simulation points (i.e., various t_{Si} for a constant t_{SiGe} or various t_{SiGe} for a constant t_{Si}). It is found that stress optimization of this entire space can be understood looking at only two variables: the ratio of t_{SiGe} to t_{Si} ($t_{\text{SiGe}}/t_{\text{Si}}$), and the aspect ratio of the Si/SiGe island ($(t_{\text{SiGe}} + t_{\text{Si}})/(2t_{\text{spacer}} + L_g)$). Fig. 7 plots the STE as a function of the aspect ratio for different $t_{\text{SiGe}}/t_{\text{Si}}$ for the range of simulation points. For each gate length, the aspect ratio space is spanned for all $t_{\text{SiGe}}/t_{\text{Si}}$ values shown. This figure shows that understanding how to maximize the STE is very simple: the values of the design variables must be chosen such that the $t_{\text{SiGe}}/t_{\text{Si}}$ ratio is as high as possible and such that the aspect ratio of the Si/SiGe island is between 0.3 and 0.5. Interestingly, the individual values of t_{SiGe} , t_{Si} , t_{spacer} , or L_g are not important themselves, only the ratios are. Using this understanding, it is very simple to determine how to design the device structure to maximize channel stress, or to determine if any particular device structure is optimized.

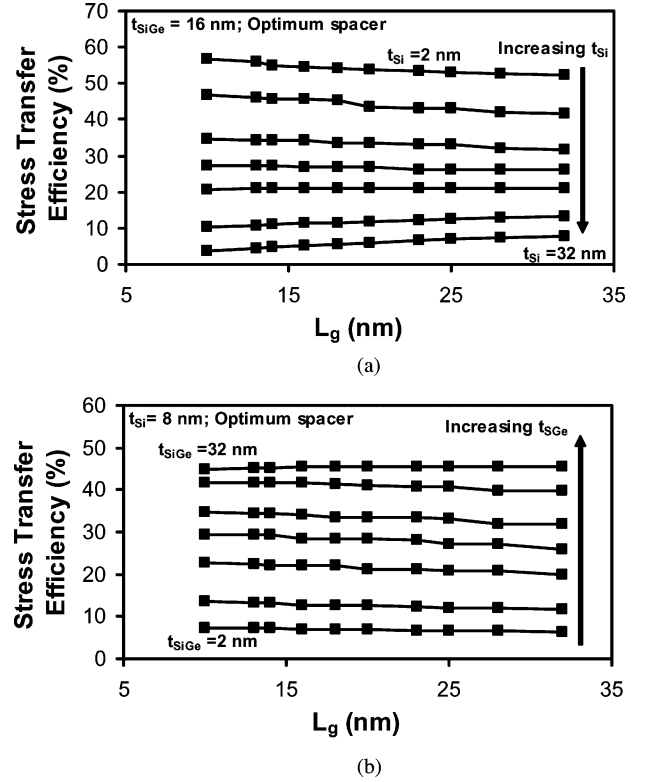


Fig. 6. Stress transfer efficiency (STE) (a) for constant t_{SiGe} and varying t_{Si} , and (b) constant t_{Si} and varying t_{SiGe} , with a wide spacer set to optimize STE. With an optimized spacer, the STE is largely independent of L_g .

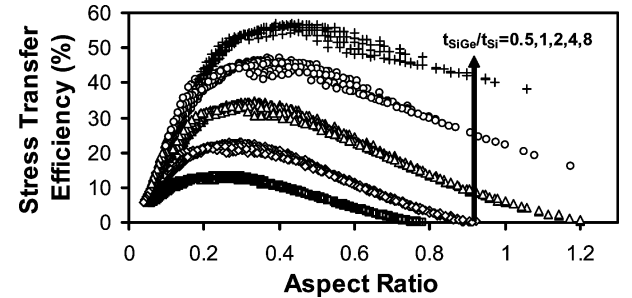


Fig. 7. Summary plot for simulation of 4900 combinations of the device parameters that determine channel stress. Optimization of the channel stress can be understood simply: the $t_{\text{SiGe}}/t_{\text{Si}}$ ratio must be maximized and the aspect ratio of the Si/SiGe island [$\text{AR} = (t_{\text{SiGe}} + t_{\text{Si}})/(2t_{\text{spacer}} + L_g)$] must be between 0.3 and 0.5.

IV. EVALUATION OF Rev. SiGe EFFECTIVENESS AND SCALABILITY

In this section, the effectiveness of the Rev. e-SiGe technique is evaluated for present-day and future CMOS nodes. First, the practical limits to the device parameters are discussed, and then, simulation of optimized device structures within these limits is presented. The stress achievable in a practical device structure is evaluated for a physical gate length between 32 and 10 nm.

The practical limit to the top silicon thickness, t_{Si} , is first discussed. The value of t_{Si} must be minimized to maximize $t_{\text{SiGe}}/t_{\text{Si}}$. The minimum practical silicon thickness is affected by the depth of the shallow source/drain extension junction ($x_{\text{jextension}}$) and the deeper contact junction (x_{jcontact}) relative

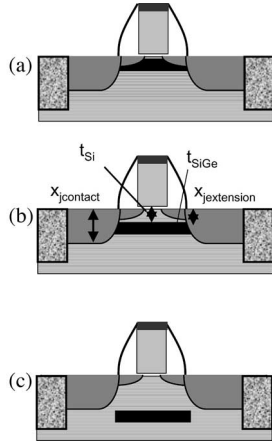


Fig. 8. Depiction of the three possible values of t_{Si} relative to $x_{jextension}$ and $x_{jcontact}$: (a) $t_{Si} < x_{jextension}$, (b) $x_{jcontact} > t_{Si} > x_{jextension}$, and (c) $t_{Si} > x_{jcontact}$.

to t_{Si} , as shown in Fig. 8. There are three possible values of t_{Si} relative to these junctions, $t_{Si} < x_{jextension}$, $x_{jcontact} > t_{Si} > x_{jextension}$, and $t_{Si} > x_{jcontact}$, as depicted in Fig. 8(a)–(c), respectively. Arsenic, the element commonly used to form the source/drain areas, has a high diffusivity in SiGe [19], and the resistance of arsenic-doped SiGe is high relative to silicon [19]. Therefore, the junction depth relative to t_{Si} has a significant impact on the extension resistance and scalability of the device. In position Fig. 8(a), in which both $x_{jextension}$ and $x_{jcontact}$ are greater than t_{Si} , the extension resistance is high because of the high resistivity of the arsenic-doped SiGe portions of the extension. The device scalability is poor because of enhanced dopant diffusion within the SiGe, worsening short-channel effects compared to a bulk silicon device [20]. In position Fig. 8(b), the extension resistance matches bulk silicon, because the extension junction does not extend into the SiGe. However, the scalability is worse than bulk silicon because of dopant diffusion from the contact diffusion toward the center of the channel into the adjacent SiGe. In position Fig. 8(c), neither junction extends into the SiGe layer; therefore, the source/drain resistance and scalability is equivalent to bulk silicon.

With these considerations in mind, it is believed that position Fig. 8(a) is not realistic because of the high source/drain resistance and poor scalability, but the other cases are believed to be plausible. Therefore, this work will analyze the last two cases: a “thin silicon” case in which $t_{Si} = x_{jextension} + 2$ nm, as in Fig. 8(b), and a “thick silicon” case in which $t_{Si} = x_{jcontact} + 2$ nm, as in Fig. 8(c), and in which the 2 nm is added to account for vertical germanium diffusion during dopant activation.

The SiGe layer thickness limit is now considered. The SiGe layer must be as thick as possible to maximize the t_{SiGe}/t_{Si} ratio. The upper bound of t_{SiGe} is limited by the formation of misfit dislocation, which will form in the SiGe to relax the layer’s compressive strain if t_{SiGe} is too large. Misfit dislocations spanning the source and drain are known to form a source/drain electrical short due to enhanced dopant diffusion along the dislocation [21]. However, the SiGe thickness limit to avoid the formation of dislocations is difficult to precisely assess. A lower bound estimate of the SiGe thickness limit is

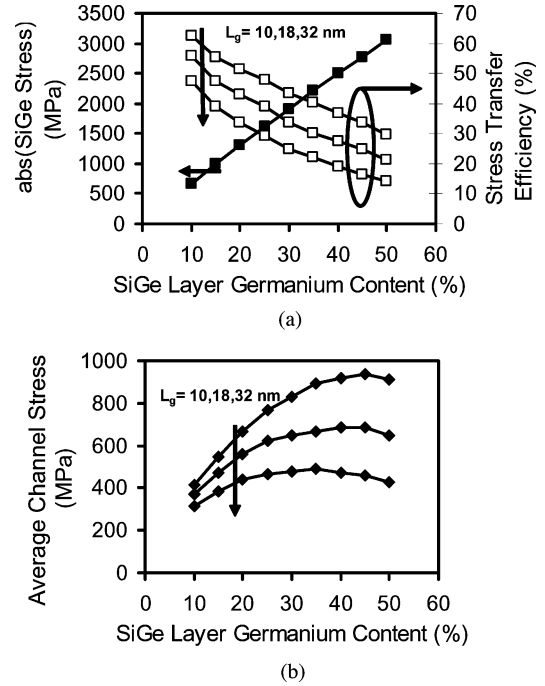


Fig. 9. Depiction of the tradeoff associated with choosing the optimal germanium fraction (and initial SiGe stress). (a) As the germanium fraction increases, the magnitude of the initial SiGe stress increases, but the STE drops. (b) The channel stress increases for small germanium fractions, but decreases for large germanium fractions. The optimum germanium fraction is around 35%. The spacer thickness was set to maximize the STE, the top silicon was thin ($t_{Si} = t_{extension} + 2$ nm), and $t_{SiGe} = 2t_{crit}$.

the equilibrium critical thickness, t_{crit} [22], the thickness at which dislocations form in the SiGe in equilibrium. However, this limit may be too conservative, as it is well known that metastable films can be grown to several times the equilibrium-critical thickness without dislocation formation if the growth temperature is low [23]. Prior work on the development of SiGe HBTs [24] has demonstrated that SiGe films up to $2t_{crit}$ can be used in a manufacturable device process. Judging from the HBT work, the maximum plausible SiGe thickness is estimated to be $4t_{crit}$, and this value is used here for the upper-bound limit on the SiGe thickness.

The limit on the SiGe buried layer stress, σ_{xx_SiGe} , is now discussed. Channel stress is directly proportional to the magnitude of σ_{xx_SiGe} ; therefore, the magnitude of σ_{xx_SiGe} should be maximized. σ_{xx_SiGe} is determined by the germanium fraction in SiGe, and therefore it would seem that the germanium fraction should be maximized. However, there is another competing factor. The critical thickness of the SiGe layer decreases as the germanium fraction increases, and therefore the allowed SiGe thickness and t_{SiGe}/t_{Si} ratio decrease, reducing the channel stress. Fig. 9 explores this tradeoff. Fig. 9(a) shows the magnitude of σ_{xx_SiGe} and the STE as a function of germanium content, and Fig. 9(b) shows the average channel stress as a function of germanium content. In these simulations, the spacer thickness was set to maximize the STE, the top silicon was thin ($t_{Si} = t_{extension} + 2$ nm), and $t_{SiGe} = 2t_{crit}$. For small germanium fractions, the channel stress increases with the germanium fraction. However, the STE falls as the germanium

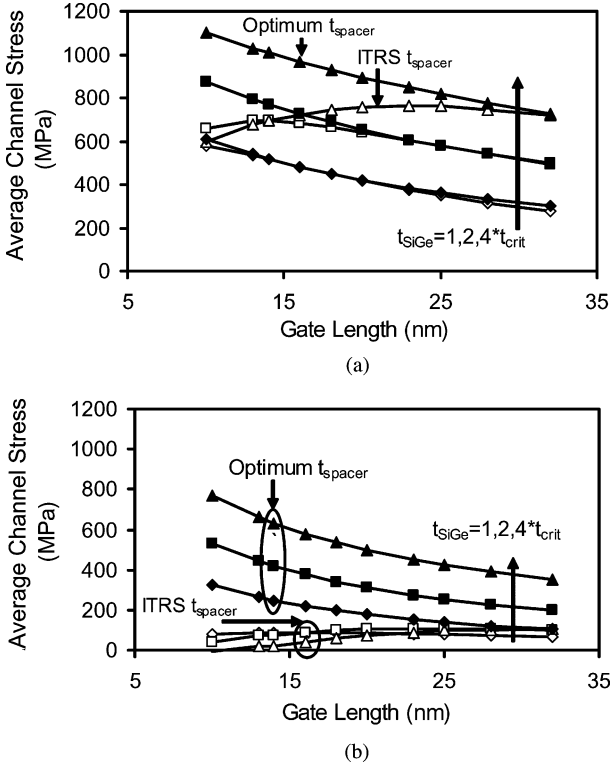


Fig. 10. Channel stress induced for realistic choices of the Rev. e-SiGe parameters. (a) The thin silicon case ($t_{Si} = x_{jextension} + 2$ nm), and (b) the thick silicon case ($t_{Si} = x_{jcontact} + 2$ nm). Ge% = 35% ($\sigma_{xx_SiGe} = -2200$ MPa).

fraction increases because the critical thickness decreases, and so the channel stress falls for a large germanium fraction. From Fig. 9, it can be seen that the channel stress is near maximum for all L_g for a germanium fraction around 35%; therefore, this germanium fraction is judged to be optimum.

Finally, the considerations involved with choosing the spacer width (t_{spacer}) are discussed. Two spacer widths are considered that span the range of plausible spacer widths: the spacer width of $1.1 \times L_g$, which will be called an ITRS spacer, and a wider, stress-optimized spacer. The device with the ITRS spacer is optimum from a source/drain resistance point of view, but not necessarily from a stress point of view, and the device with a stress-optimized spacer is optimum from stress point of view, but not from a source/drain resistance point of view.

Using the practical limits on t_{SiGe} , t_{Si} , σ_{xx_SiGe} , and t_{spacer} defined earlier, the effectiveness of Rev. e-SiGe technology is now evaluated as a function of L_g . Fig. 10(a) and (b) shows the average channel stress for thin silicon ($t_{Si} = x_{jextension} + 2$ nm) and thick silicon ($t_{Si} = x_{jcontact} + 2$ nm), respectively. The other parameters were set as follows: $\sigma_{xx_SiGe} = -2200$ MPa (Ge% = 35%); $t_{spacer} =$ ITRS or stress optimized, $t_{SiGe} = t_{crit}, 2t_{crit}$, or $4t_{crit}$. The $x_{jextension}$ is set to $L_g/3$, $x_{jcontact} = 1.1 \times L_g$, and $t_{spacer} = 1.1 \times L_g$, as prescribed by the ITRS [15], and t_{crit} is set to 7.5 nm for Ge% = 35% from [22].

Several clear conclusions can be made from the thin silicon simulations shown in Fig. 10(a). It is highly beneficial for the compressed SiGe to exceed the critical thickness in most cases. For example, for $L_g = 18$ nm, the average channel stress in-

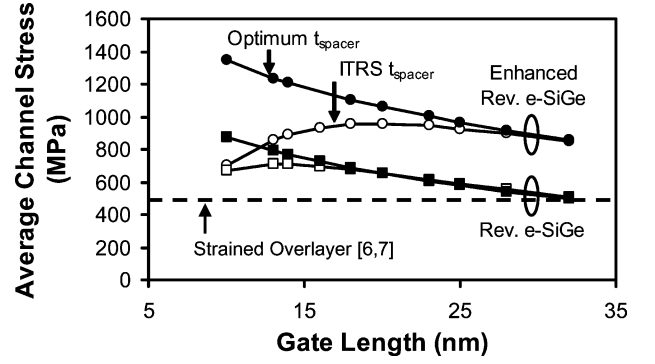


Fig. 11. Channel stress for realistic choices of the critical parameters for a conventional strained overlayer process [6], [7] and the enhanced and standard Rev. e-SiGe processes. The standard Rev. e-SiGe process produces a similar stress level to the conventional technique at $L_g = 32$ nm and is scalable. The enhanced process induces significantly higher stress levels for most L_g . The use of optimized spacers is needed to maintain the stress advantage for the smallest L_g . $t_{SiGe} = 2t_{crit}$, thin t_{Si} ($t_{Si} = x_{jextension} + 2$ nm), Ge% = 35% ($\sigma_{xx_SiGe} = -2200$ MPa).

creases from 450 MPa for $t_{SiGe} = t_{crit}$ to about 950 MPa for $t_{SiGe} = 4 \times t_{crit}$. The figure also shows that the stress increases with decreasing gate length in most cases. This is due to the reduction of $x_{jextension}$ (and therefore, t_{Si}), which is coupled to the reduction of the gate length. Fig. 10(a) shows that ITRS spacers are effective in most cases, but that wider, stress-optimized spacers are beneficial when the SiGe is thick and the gate length is small.

Fig. 10(b) shows the simulation results for the thick silicon case. The channel stress is significantly lower for thick silicon because the t_{SiGe}/t_{Si} ratio is smaller. Using the wide, stress-optimized spacers is necessary to induce significant stress levels in all the cases.

It is now possible to compare a realistic Rev. e-SiGe device to a conventional strained-silicon device. Fig. 11 shows the average channel stress for one of the practical device structures simulated earlier, chosen to be representative of the Rev. e-SiGe technique. The chosen device has thin silicon, $\sigma_{xx_SiGe} = -2200$ MPa (Ge% = 35%), t_{SiGe} of $2t_{crit}$, and with ITRS or stress-optimized spacers. Fig. 11 also shows the stress level induced by a strained nitride capping layer, a common conventional NMOS strained-silicon technique [6], [7]. The Rev. e-SiGe technique induces a similar stress level to the conventional technique, 500 MPa, at an L_g of 32 nm. With ITRS spacers, the stress increases with L_g scaling to 670 MPa at $L_g = 18$ nm. Scaling further to $L_g = 10$ nm results in no further stress increase with ITRS spacers, but the stress can be increased to almost 900 MPa at an L_g of 10 nm using stress-optimized spacers. Fig. 11 also shows the stress induced using an enhanced Rev. e-SiGe process, and this process is described in the next section.

V. DESCRIPTION AND EVALUATION OF AN ENHANCED Rev. e-SiGe PROCESS

This section describes a modification to the Rev. e-SiGe process that significantly enhances its effectiveness. The modified process is first described, and then simulations are used to examine the channel stress induced by the enhanced process. It is

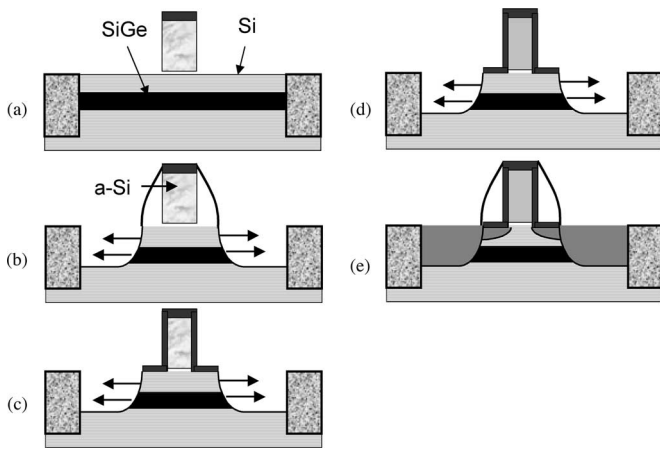


Fig. 12. Enhanced Rev. e-SiGe process designed to create a quasi-free surface above the silicon channel, which can increase the channel stress significantly for a given device structure. (a) After STI, the Si/SiGe layers are grown and the gate deposition and etch process is completed. (b) The gate material is amorphous silicon. Etching the source/drain creates a lateral free surface, allowing the SiGe and silicon to expand. (c) Spacer removal and (d) gate recrystallization, creates a quasi-free surface on top of the channel allowing the SiGe and silicon layers to expand further. (e) The CMOS process is completed.

shown that the enhanced process can substantially increase the STE of a device structure.

An examination of the Rev. e-SiGe technique reveals that the gate and spacer have an undesired effect on the channel stress. The gate and the spacers constrain the expansion of the SiGe and top silicon layer after the source/drain etch step. Tensile stress is transferred into the gate and the spacers as well as to the channel, as can be seen in Fig. 2(b), reducing the tensile stress transferred to the channel. Therefore, the STE of a Rev. e-SiGe device can be improved if the physical constraints imposed by the gate and spacers can be eliminated. It is clear, however, that simply removing the gate and the spacers is not a useful solution, as they perform a necessary function in the operation of a MOSFET.

It may be possible to eliminate the effect of the gate and spacer from a stress point of view, however, and one fabrication process to accomplish this is now proposed. Fig. 12 describes an enhanced Rev. e-SiGe fabrication process starting after the STI process. The SiGe and silicon layers are selectively grown on the NMOS islands, the gate oxide is grown, and the gate material is deposited and etched [Fig. 12(a)]. In this process, amorphous silicon is used as the gate material, different from the polysilicon used in the standard process. Oxide spacers with a nitride liner are then deposited and etched [Fig. 12(b)]. The source/drains are next etched to create a lateral free surface and allow the SiGe to expand [Fig. 12(b)]. Next, the spacers are etched away [Fig. 12(c)], and then, the wafer is annealed to recrystallize the amorphous gate material, which allows the stress in the gate to relax [Fig. 12(d)]. In effect, a quasi-free surface is created on top of the silicon layer. The spacer etch and recrystallization process steps increase the relaxation of the SiGe layer and increase the stress transfer to the top silicon layer. Although these two process steps have never been suggested for the Rev. e-SiGe structure, they have been separately demonstrated in standard CMOS processes. The first step has

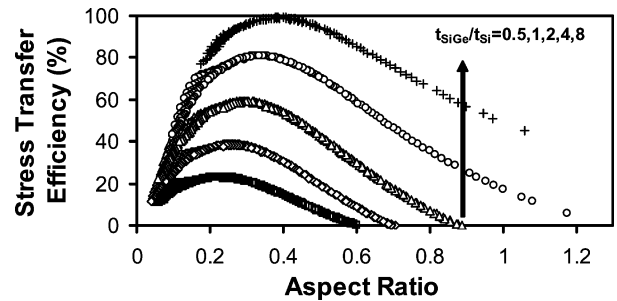


Fig. 13. Summary plot for the simulation of the enhanced Rev. e-SiGe process for 4900 combinations of the device parameters. Optimization of the channel stress can be understood simply in the same way as the standard Rev. e-SiGe process. Comparing this figure to Fig. 7 shows that the enhanced process induces significantly more stress than the standard Rev. e-SiGe process for most device structures.

been done in a CMOS process with spacer removal [7], [8], and the second is part of the stress memorization technique [9]–[11].

The enhanced process was simulated for the entire range of critical variables to produce a plot similar to Fig. 7 for the enhanced device structure, and this plot is shown in Fig. 13. The simulations were done for the idealized case of a completely free top surface; the realistic enhanced process approaches the idealized case at the limit of an infinitely thin nitride liner. The STE for the enhanced Rev. e-SiGe process is significantly higher than that for the basic Rev. e-SiGe process for a given $t_{\text{SiGe}}/t_{\text{Si}}$ and aspect ratio. For example, for the optimum aspect ratio and a $t_{\text{SiGe}}/t_{\text{Si}}$ ratio of 2, the STE increases from 30% for the basic process to 60% for the enhanced process.

The effectiveness of the enhanced Rev. e-SiGe structure for realistic choices of the critical variables is compared to the standard Rev. e-SiGe structure in Fig. 11. The enhanced Rev. e-SiGe technique induces significantly higher stress levels in many cases. The enhanced Rev. e-SiGe structure is very effective for $L_g = 32$ nm, increasing the stress from 500 to 850 MPa, a 70% increase, significantly higher than the conventional strained nitride cap technique. The effectiveness of the enhanced Rev. e-SiGe with ITRS spacers is largely maintained at $L_g = 18$ nm. For the shortest L_g of 10 nm, the enhanced technique is not effective unless the stress-optimized spacers are used, in which case nearly 1400 MPa of stress is induced in the channel.

VI. CONCLUSION

An extensive simulation study of reverse embedded-SiGe, a promising new NMOSFET strained-silicon technique, is described. Thorough stress simulations were executed involving 4900 combinations of the critical determinants of channel stress. This paper makes several important contributions toward understanding and evaluating the Rev. e-SiGe technique. First, it shows that optimization of the device structure to maximize channel stress can be understood simply using only two underlying variables, the $t_{\text{SiGe}}/t_{\text{Si}}$ ratio and the Si/SiGe island aspect ratio. Second, it presents a study of the channel stress achievable in realistic, optimized device structures. It shows that realistic devices can induce a stress level comparable to or exceeding a conventional strained-silicon process. Furthermore, it shows that

the Rev. e-SiGe structure is scalable: the channel stress is maintained as gate length is scaled down from 32 to 10 nm with an ITRS spacer, and the stress increases substantially with scaling if the spacer width is optimized. Third, an enhanced Rev. e-SiGe process is proposed involving spacer removal and gate recrystallization. The enhanced process can nearly double the channel stress relative to the standard Rev. e-SiGe technique. This work substantially advances the state-of-the-art understanding of the Rev. e-SiGe technique, and it is hoped that it will ultimately contribute to the continued progress of CMOS technology.

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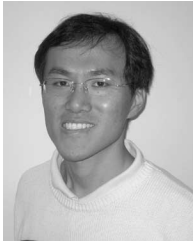
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