Stress Simulation of a Germanium Reverse Embedded-SiGe PMOSFET

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Germanium channel MOSFETs are among the most attractive candidates for performance enhancement in future CMOS nodes. Strained Ge PMOSFETs are particularly promising and have a theoretical mobility enhancement of up to 20x [1] relative to silicon for practical levels of strain. Several strain technologies have been demonstrated for Ge PMOSFETs, including the growth of thin layers of Ge directly on silicon [2], and the growth of Ge on a Si_xGe_{1-x} graded buffer [3]. These technologies apply compressive biaxial strain to the channel. However, modeling [1] and wafer bending experiments [4] suggest that uniaxial longitudinal stress may be more effective than biaxial stress in Ge PMOSFETs, similar to silicon PMOSFETs. Unfortunately, the embedded SiGe source/drain process used for silicon PMOSFETs [5] can't be used to apply compressive strain to Ge PMOSFETs.

Here we describe a uniaxial compressive strain technique for Ge channel PMOSFETs. We show, using simulations, that the recently demonstrated silicon reverse embedded-SiGe technique (Rev. e-SiGe) [6-8] can be easily adapted for this purpose.

A fabrication process for a Ge channel Rev. e-SiGe PMOSFET is outlined in Fig. 1. The fabrication process is essentially identical to that of the silicon Rev. e-SiGe NMOSFET, except that the device is created on Ge instead of silicon. 2-D TSUPREM4 simulations of the stress in the Ge Rev. e-SiGe structure are shown in Fig. 2. Fig. 3 plots the longitudinal stress (σ_{xx}) through the center of the gate and into the substrate for a Ge Rev. e-SiGe device, and this can be compared to the same profile for a Si Rev. e-SiGe device in Fig. 4. Stress values in the Ge device are similar to those in the Si device *except that the sign of the stress is reversed*. In the Ge device, the buried SiGe layer is initially in tension. The source/drain etch reduces this stress and transfers compressive stress to the Ge channel, making the technique useful for Ge PMOSFETs. Conversely, in the Si device the buried SiGe layer is initially under compression, and the etch transfers tensile stress to the channel, making the technique useful for Si NMOSFETs.

Fig. 5 demonstrates the promise of the Rev. e-SiGe technique for straining Ge devices in future CMOS nodes. This figure shows the average channel stress under the gate at the Ge/insulator interface for realistic choices of the device structural characteristics. A high level of channel stress is produced for gate lengths down to 10 nm.

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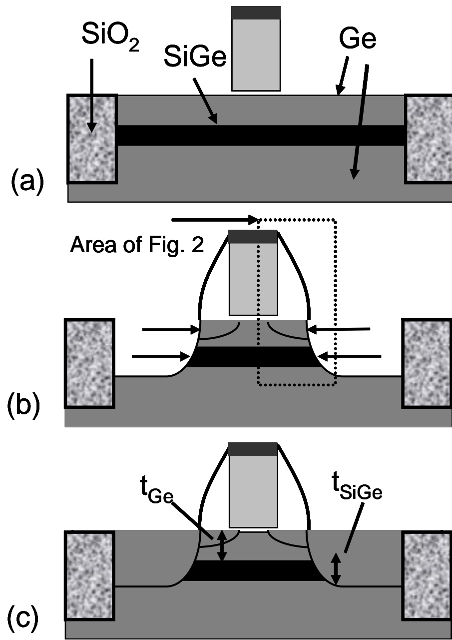

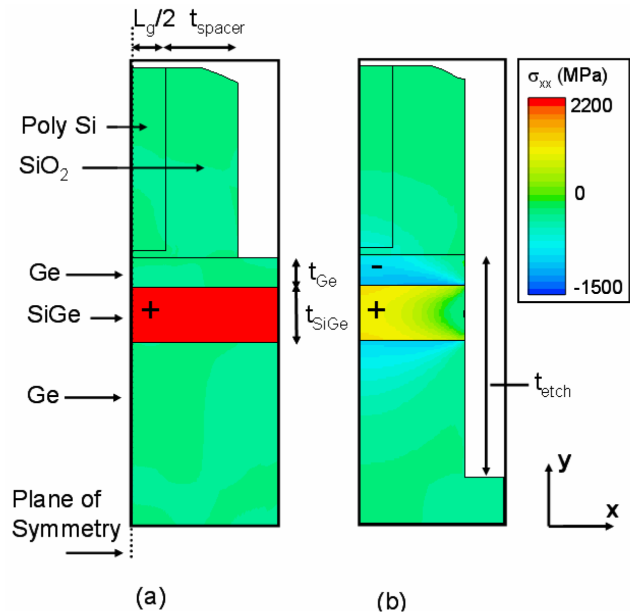

Fig. 1 Outline of Ge Rev. e-SiGe PMOSFET fabrication process. After the device isolation, a recess is etched and thin layers of SiGe and Ge are grown (Fig. 1a). The gate and spacers are made and then the source/drain regions are etched (Fig. 1b). Germanium is re-grown in the source/drain regions (Fig. 1c).

Fig. 2 TSUPREM4 simulations of stress before (a) and after (b) etch of the source/drain. The source/drain etch allows the buried SiGe layer to contract, inducing compressive stress in the overlying germanium channel. Initial SiGe stress is 2200 MPa ($Si_{0.37}Ge_{0.63}$), L_g = 18 nm, t_{spacer} = 20 nm, t_{Ge} = 8 nm, t_{SiGe} = 15 nm, and t_{etch} = 60 nm.

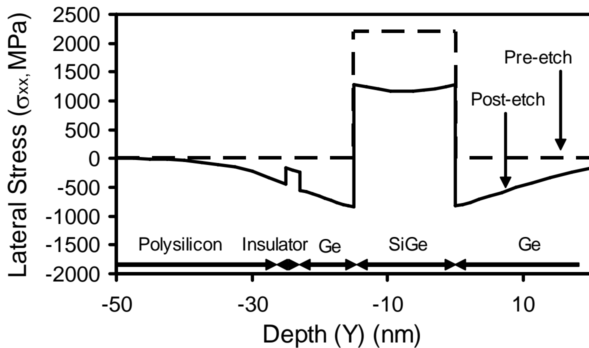

Fig. 3 Stress profile through the center of the gate for the Ge Rev. e-SiGe device in Fig. 2. Compressive stress is induced in the channel by relaxation of the tensile stress in the SiGe. Stress at the Ge surface is -550 MPa.

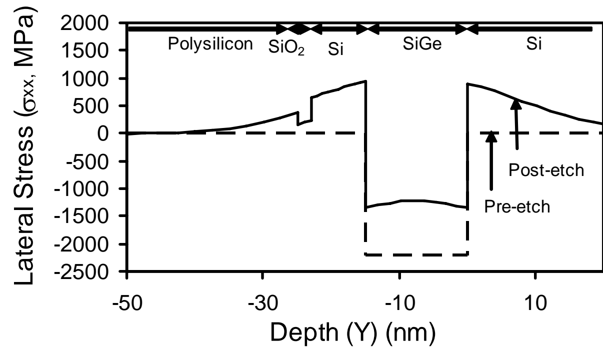

Fig. 4 Stress profile through the center of the gate for a Si Rev. e-SiGe device [8]. The device dimensions are the same as Fig. 2 and Fig. 3, except that the initial SiGe stress is -2200 MPa. Tensile stress is induced in the channel.

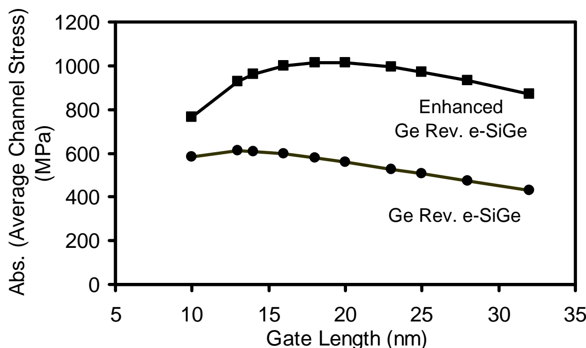

Fig. 5 Average compressive stress beneath the gate for realistic choices of device structural characteristics. Initial SiGe stress = 2200 MPa ($Si_{0.37}Ge_{0.63}$), t_{SiGe} = 15 nm. t_{spacer}, was set according to ITRS projections for each L_g (i.e. $t_{spacer} = 1.1*L_g$). t_{Ge} set to $x_{jextension}$ + 2 nm, $x_{jextension}$ was set according to the ITRS for each L_g. The enhanced process simulates the idealized case of a completely free Ge top surface (see [8]). The Rev. e-SiGe technique is effective at inducing a high uniaxial compressive stress level in the Ge channel for small L_g.