Aspect Ratio Trapping, a New Approach to Heteroepitaxy of Ge and III-Vs on Si

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Heteroepitaxy of Ge and III-Vs on Si is of great importance for the integration of optoelectronic devices with Si and for future high performance CMOS as well. For these applications, a dramatic reduction of dislocation density as high as 10^8-10^9 cm^{-2} is critical. In addition, a solution needing minimal epi thickness and minimal thermal budget, for the ease of integration with Si CMOS, is highly desirable. In this paper we review a new approach, referred to as Aspect Ratio Trapping (ART), which satisfies these requirements, and which relies only upon conventional steps in common use in Si CMOS manufacturing. We demonstrate effective trapping of threading dislocations of Ge and GaAs in trenches of arbitrary length, using epilayers as thin as 450 nm, selectively grown in SiO_2 trenches with aspect ratio (AR) > 1. We evaluate the mechanisms of the reduction in defects, and demonstrate planarized SiGe and Ge ART structures suitable for device applications.

Cross-sectional transmission electron microscope (TEM) images of Ge in trenches [Figs. 1(a)-1(b)] show that the dislocations originating at the Ge/Si interface terminate at the oxide sidewall well below the Ge surface, in trenches of 200 nm (AR=2.5) width and 400 nm (AR=1.2) width [1]. Plan-view imaging [Fig. 1(c)] also shows the termination of dislocations at the sidewall; defect-free Ge is demonstrated after removing the dislocation trapping region by thinning the TEM sample further [Fig. 1(d)]. Defect-free GaAs in trenches was also demonstrated in the same way, as shown in Fig. 2 [2]. Fig. 3(a) shows Ge grown with $Si_{0.9}Ge_{0.1}$ marker layers, which serve to delineate the evolution of the epitaxial surface. Threading dislocation segments roughly follow the local facet normal, and hence are effectively guided toward the sidewalls, promoting trapping, and this clearly exhibits so-called “growth dislocation” behavior [3]. Coalesced Ge layers have been formed by lateral epitaxial growth over sidewall regions, which results in the generation of dislocations and voids as shown in Fig. 3(b) [4]. Non-coalesced regions of SiGe and Ge, co-planar with the surrounding SiO_2 isolation, have been produced via chemical-mechanical polishing [Fig. 4(b) and 4(d)]. These low-defect epi-regions could be utilized, for example, for a strained-Ge PFET device [Fig. 4(a)], or for a Ge tri-gate FET [Fig. 4(c)].

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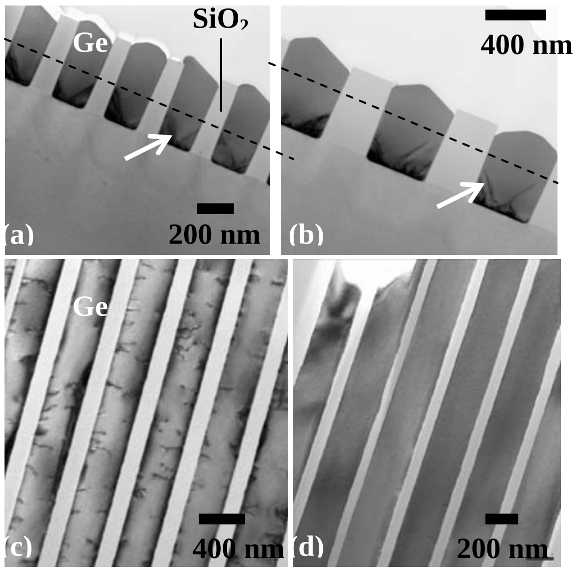

Fig. 1 XTEM images of Ge in trenches of (a) 200 nm width and (b) 400 nm width and PVTEM image of Ge in trenches (c) with the trapping evident and (d) with the sample thinned further to remove the defect trapping region. The dashed lines in (a) and (b) indicate where AR=1 [1].

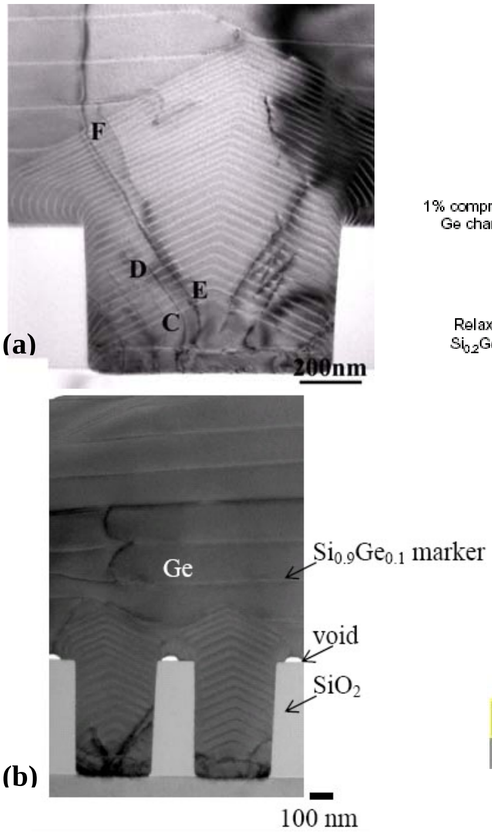

Fig. 3 (a) XTEM image of Ge with $Si_{0.9}Ge_{0.1}$ marker layers in trenches of 800 nm width showing the redirection of threading dislocations under the influence of faceting [3] (AR here is not sufficient for full trapping) and (b) coalesced Ge in trenches of 375 nm width [4].

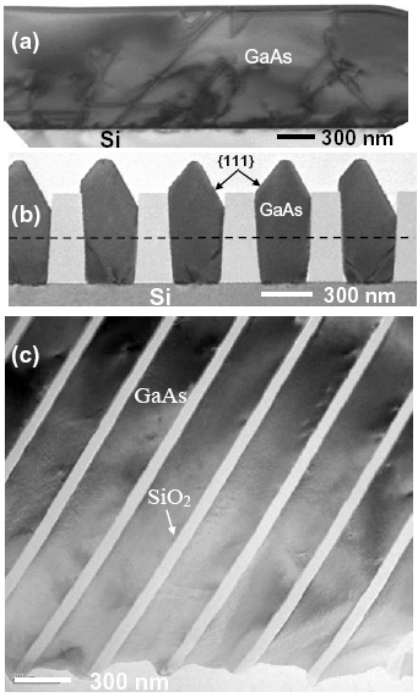

Fig. 2 XTEM images of GaAs (a) on blanket Si(001) and (b) in trenches showing defect trapping and (c) PVTEM image of GaAs in trenches of 290 nm width. For the thinnest portion of this wedge-shaped sample near the image bottom, the defect trapping region has been removed [2].

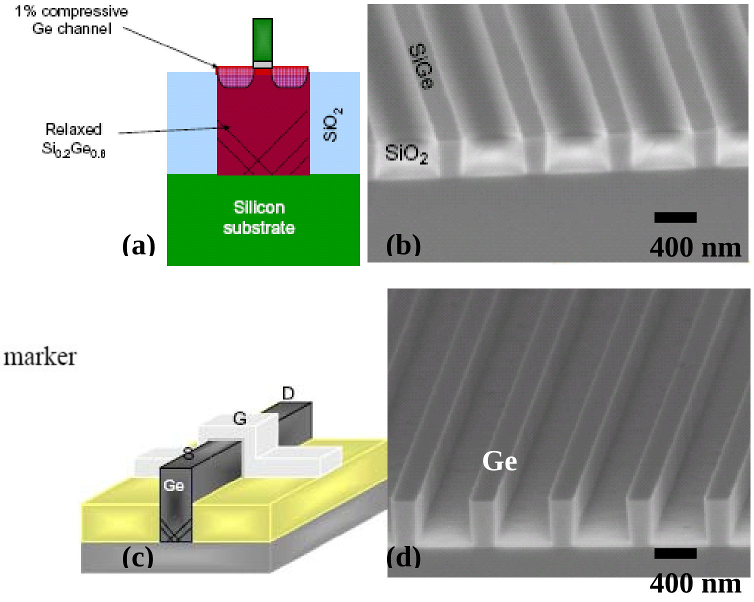

Fig. 4 (a) Schematic of proposed strained-Ge channel FET on relaxed $Si_{0.2}Ge_{0.8}$ grown via ART. (b) SEM image of $Si_{0.2}Ge_{0.8}$ in trenches after CMP, (c) schematic of proposed tri-gate FET using Ge ART with subsequent reduction of SiO_2 sidewall height. (d) SEM image of Ge in trenches after CMP and oxide removal using a dilute HF.