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Defect reduction of GaAs/Si epitaxy by aspect ratio trapping

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We report on the metallorganic chemical vapor deposition growth of GaAs on patterned Si (001) substrates, which utilizes the aspect ratio trapping method. It was found that when growing GaAs above the SiO_2 trenched region, coalescence-induced threading dislocations and stacking faults originated on top of the GaAs/SiO_2 interfaces. These defects were found to be indirectly related to the initial defect-trapping process during trenched GaAs growth. Causes of coalescence defect formation and its reduction were experimentally investigated by employing a two-step growth optimization scheme. Improvement of material quality has been characterized by cross-sectional and plan-view transmission electron microscopy and x-ray diffraction. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2924410]

Selective epitaxy of GaAs on Si substrates patterned with dielectric films has been studied for many years and significant improvements of film quality have been reported.[1–8] However, a process with consistently low threading dislocation density (TDD) has not been demonstrated. Recently, we demonstrated defect-free Ge and GaAs regions grown in SiO_2 trenches directly on Si substrates via the aspect ratio trapping (ART) method,[9,10] whereby TDs arising from lattice mismatch are trapped at vertical sidewalls confining the growth region. As part of this continuing investigation, we show here recent progress on producing continuous GaAs films on SiO_2-patterned Si substrates. The film quality has been analyzed via transmission electron microscopy (TEM) and x-ray diffraction (XRD) and compared to similar growth on unpatterned Si substrates. Significant reduction in TDD and in XRD full width at half maximum (FWHM) have been obtained within a total epithickness of less than 1.5 μm. These results were obtained on 200 mm Si wafers with processes compatible with Si industry fabrication, which suggest an eventual pathway to III–V devices monolithically integrated with Si complementary metal oxide semiconductor.

The substrates used in this study were *n*-type Si (001). Process details of SiO_2 mask patterning and substrate cleaning were as previously described.[10] To understand the various defect formation mechanisms, a two-step epitaxy process was used in this study. In the first step, GaAs was grown inside the SiO_2 trench confined region without coalescence. The formation of defects inside the trenches and their regulation by the ART process was analyzed in this step, In the second step the GaAs layer was grown above the SiO_2 film and coalesced. Here, the investigation focused on the coalescence-related defects.

Initial experimentation was performed on the growth and optimization of bulk GaAs films on blanket Si substrates. A desirable film quality was achieved on the planar Si substrates with XRD FWHM about 300 arcsec ($\omega/2\theta$) for a 1.5 μm GaAs film. This process served as a baseline during studies with SiO_2-patterned substrates. Furthermore, a blanket Si control wafer was always used in conjunction with each patterned wafer growth to monitor the growth condition drift. During the first step of the growth, studies focused on decreasing TDD, minimizing trapping layer thickness, and eliminating planar defects originating at the SiO_2 sidewalls. Characteristics of the resulting epiregions were found to be sensitively related to the pregrowth, bake-step temperature, the buffer layer thickness, the top layer growth temperature, and the V/III ratio. Figure 1 shows cross-sectional TEM image of GaAs layers within trenches having a width of 0.27 μm and corresponding aspect ratios (trench height/trench width) of 1.8. It can be seen that dislocations originating at the GaAs/Si interface are completely terminated within the first 200 nm of GaAs growth; this is indicated by the dashed line in Fig. 1. As a result, a defect-free region is created as the growth proceeds beyond the defect-trapping region.[10]

Initial coalesced GaAs growth was performed by using the above mentioned growth conditions with the addition of an increased growth time for the top layer to obtain a continuous film above the trenches. A typical cross-sectional TEM image is shown in Fig. 2(a). At the lower portion of the trenched area, the defect trapping essentially occurs in the same manner as that of the uncoalesced GaAs layer. However, many new dislocations appeared starting from the top surface of the SiO_2 mask. Also, planar defects were observed at the upper portion in between dielectric masks. Experimen-

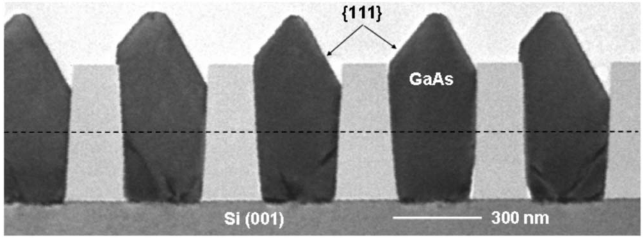

FIG. 1. Cross-sectional TEM image of GaAs grown on ART patterned Si.

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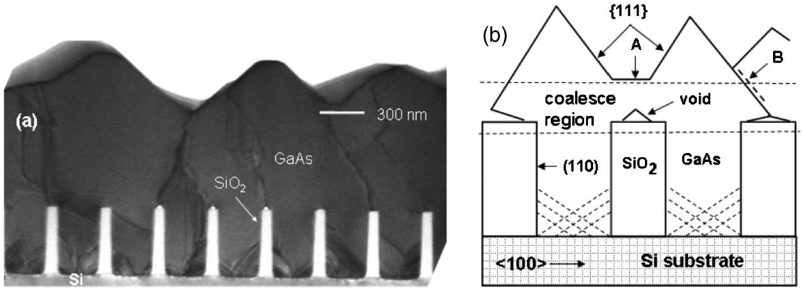

FIG. 2. Cross-sectional TEM image of (a) coalesced GaAs grown under the same growth conditions as for Fig. 1(a). (b) Schematic illustration of coalesced GaAs growth.

tal investigations were conducted to modify initial growth conditions but no improvement was observed. It is, therefore, likely that the coalescence defects have different formation mechanisms from those observed during the trenched GaAs growth. In other words, the growth processes developed for defect-trapping remain to be effective only prior to coalescence. Another feature observed in Fig. 2 is the rough crystallographic surface. This is related to the epilayer thickness after coalesced growth.

Figure 2(b) is a schematic model illustrating coalesced GsAs growth via ART. When GaAs grow near the top of the trenches, triangular cross sections are observed with sides defined by {111} facets, as shown in Fig. 1(a). As growth on these facets proceeds, the surfaces of these trench-length GaAs wedges extend toward each other over the SiO_2 separator. A (001) surface is then presumed to form, which bridges the gap between adjacent trenches, labeled A in Fig. 2(b). The GaAs layer in between the two dashed lines is the “coalesced layer” with a thickness of about 100–200 nm. A void often remains in the coalescence region, as can be seen in the TEM images of Fig. 2(a).

We have found, in general, that the quality and smoothness of this coalesced GsAs layer are highly sensitive to growth conditions. Hard-to-control asymmetries and irregularities of faceted growth regions prior to coalescence (as seen in Fig. 1) may be leading to elevated defect density in the coalescence regions and heightened roughness in the resulting film. In comparison, the quality of the GaAs growth inside the trenches is less sensitive to growth conditions. The coalescence-induced defects typically appear in the form of twin defects, microstacking faults, or their combinations. These are often initially inclined toward {111} facets and thread into the upper layer as growth proceeds, as marked with letter B in Fig. 2(b). The key focus in the remainder of this report is reducing such “coalescence defects.”

Based on the above analysis and the earlier reported trench growth results, we optimized the growth parameters specifically for the coalesced growth region. Figure 2(b) suggested that an optimization of the wedge-shaped surface morphology is beneficial to coalescence formation. In other words, prior to coalescence, a uniform and symmetric array of GaAs{111} facets is desirable. This was accomplished in this study by initiating growth mode parameters for coalescence growth when growth of the GaAs was still about 50 nm lower than the top of the SiO_2 trench surface. This is indicated by the position of the lower dashed line in Fig. 2(b). Also, it has been reported that lower growth pressure and higher growth temperature improve selective growth morphology,[11] while lower growth temperature and higher V/III ratio are helpful for reducing microtwin defects.[12] However, our low-pressure GsAs grown in the trenches yielded higher twin defects. To optimize the competing growth parameters, we maintained growth pressure at 70 torr but chose 650 °C as the growth temperature for the coalesced layer, which was 30 °C lower than its neighboring layer growth temperature. In addition, we reduced the growth rate to half of the regular value and doubled the V/III ratio during coalesce layer growth.

Figure 3 shows the cross-sectional TEM image of the growth result. It is evident that in the region above the SiO_2, defects were significantly reduced in comparison with the unoptimized growth results seen in Fig. 2(a). Despite the presence of some tilted defects above the trenched region, there is essentially no new defects that appear to be generated in the upper region. This result implies that a well-optimized multistep growth process may lead to complete trapping of TDs inside the SiO_2 trenches. Further understanding and improved process control study should yield additional improvements.

Figure 4 shows x-ray measurement results of the sample in Fig. 3. XRD was conducted on ART patterned Si wafer with a Philips X’Pert Pro Materials Research diffractometer. The FWHM of ω scan for the film is 190 in., which appears among the low records of FWHM of metal-organic chemical vapor deposition grown GsAs on Si with thickness of less than 1.5 μm.[13,14]

In summary, two-step growth optimization has been applied to GaAs epitaxy on Si substrates with trenches patterned through SiO_2 layers. It confirmed that the optimal ART method yields defect-free bulk GaAs regions grown inside the trenches. However, a delicate second-step growth optimization step is required to reduce the coalescence-induced defects for growth of continuous films. The results

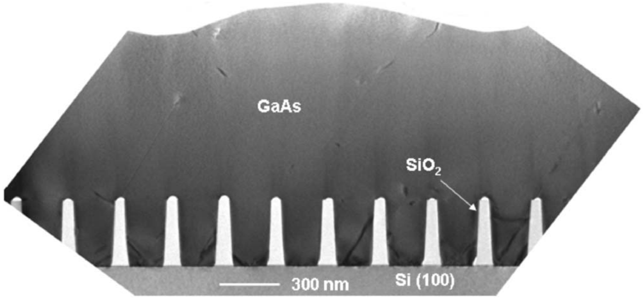

FIG. 3. Coalesced GaAs grown under optimized growth conditions by using two-step defect-trapping method.

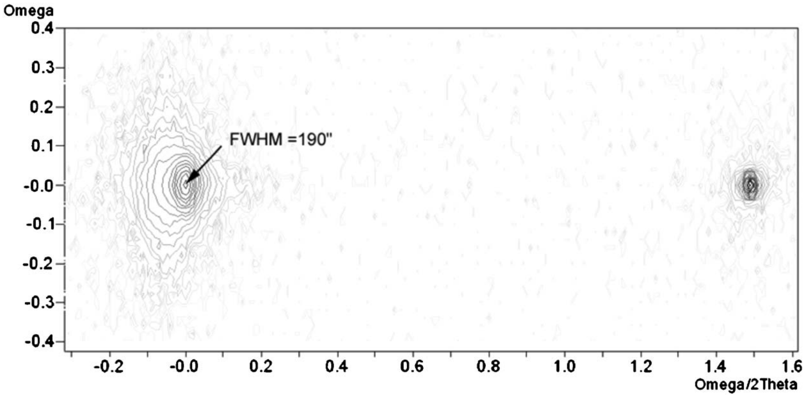

FIG. 4. Reciprocal space map of the (004) plane x-ray reflection of coalesced GaAs grown on an ART patterned Si substrate.

indicate that all of the defects resulting from the GaAs/Si lattice mismatch can potentially be suppressed by the ART structure layer through proper multistep growth optimization. This approach shows great promise for developing high quality GaAs and other III–V compound materials by using Si substrates.

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