Defect Reduction and Its Mechanism for Selective Ge Epitaxy on Si(001) Using Aspect Ratio Trapping (ART™)

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Integrating Ge or III-V with Si CMOS

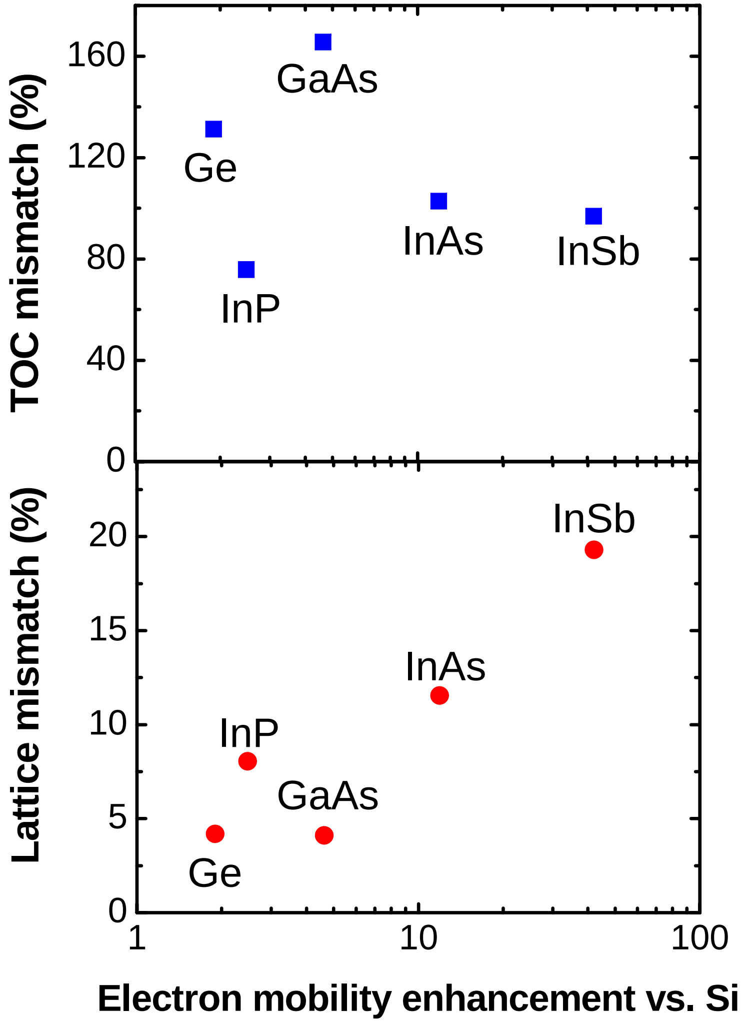
Why Ge or III-V on Si?

Three key areas:

- Improve economics for existing III-V applications
- Add new functionality to Si CMOS platform
- Replace Si for CMOS channel

Key Challenges

- *Lattice mismatch*
- *Thermal expansion coefficient (TOC) mismatch*



Integrating Ge or III-V with Si CMOS

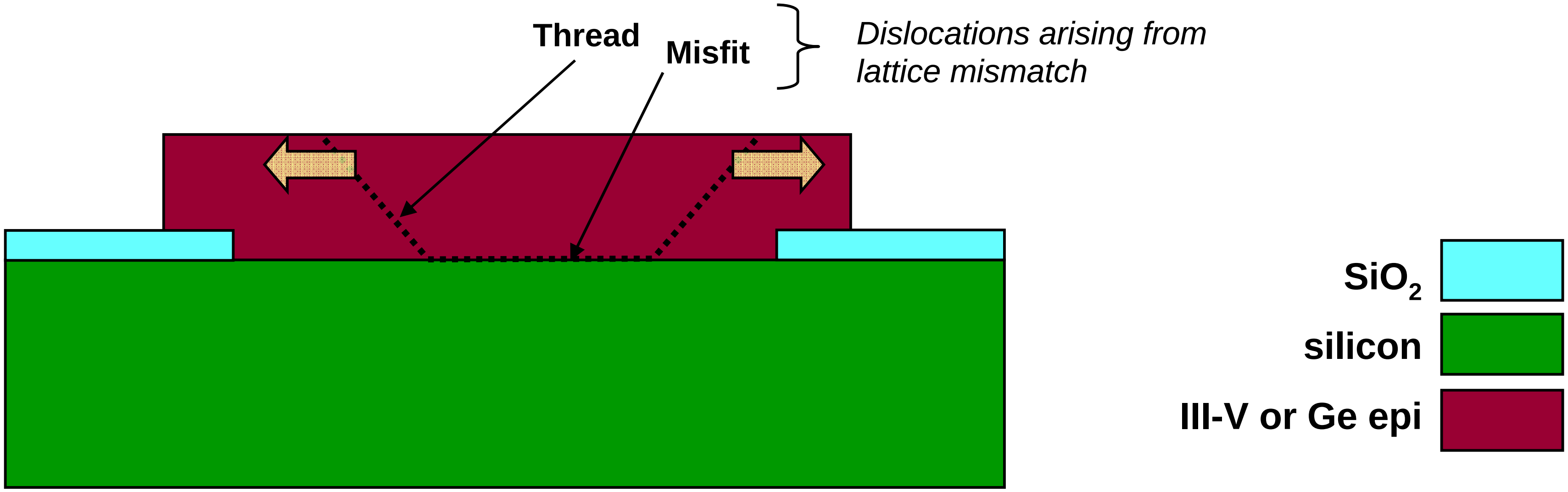
Ideal solution should:

- Control threading dislocation density
- Avoid thick epitaxial layers
  - Minimize TOC mismatch stress
- Avoid aggressive thermal anneals
- Put non-Si material only where it's needed

For CMOS compatibility

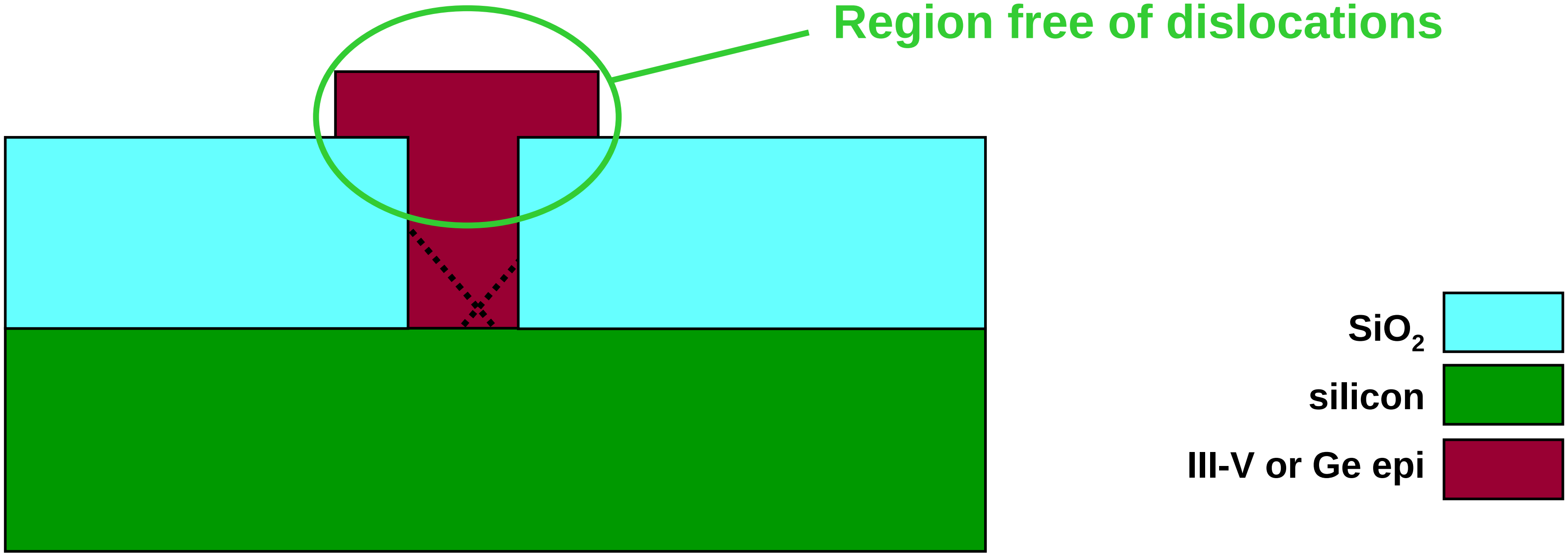
Can these criteria be met by hetero-epitaxial growth?

- Researched by various groups, late ‘80s onward
- Strain tends to drive dislocations toward pattern edges, where they can exit the epi island



- **However, there are severe limitations:**
  - Can only work for glissile (mobile) dislocations
    - Sessile (immobile) dislocations dominate for > 2% lattice mismatch
  - Dislocation interactions typically pin even glissile dislocations

Modified approach: “Aspect Ratio Trapping” (ART)



- **Geometry of dislocations in cubic semiconductors allows trapping by sidewalls, with sufficient aspect ratio (h/w)**
- **Has been explained as “epitaxial necking”**
  - E. Fitzgerald et al., J. Electron. Mater. **20**, 839 (1991)
  - T. Langdo et al., Appl. Phys. Lett. **76**, 3700 (2000)

Outline

- Experimental conditions
- XTEM and XRD results
- Investigation of trapping mechanism
- Conclusion

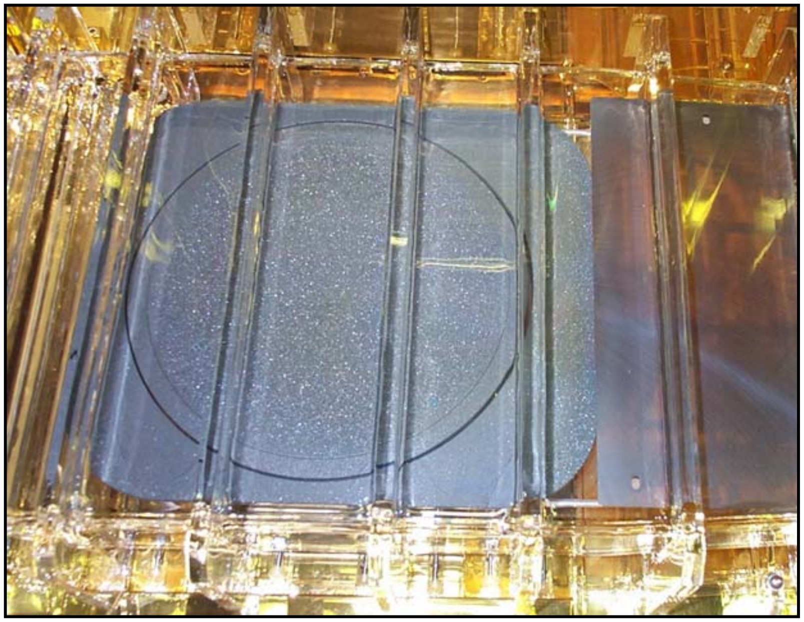
Wafer Preparation

- 500 nm thermal SiO_2 mask grown on 8” wafers
- Trench patterning in 248 nm stepper
- Oxide RIE stopping selectively in Si
- Plasma ash (800 W, 20 min) to remove fluorocarbon residue from RIE
- Post RIE clean: Piranha, SC2, and dilute HF

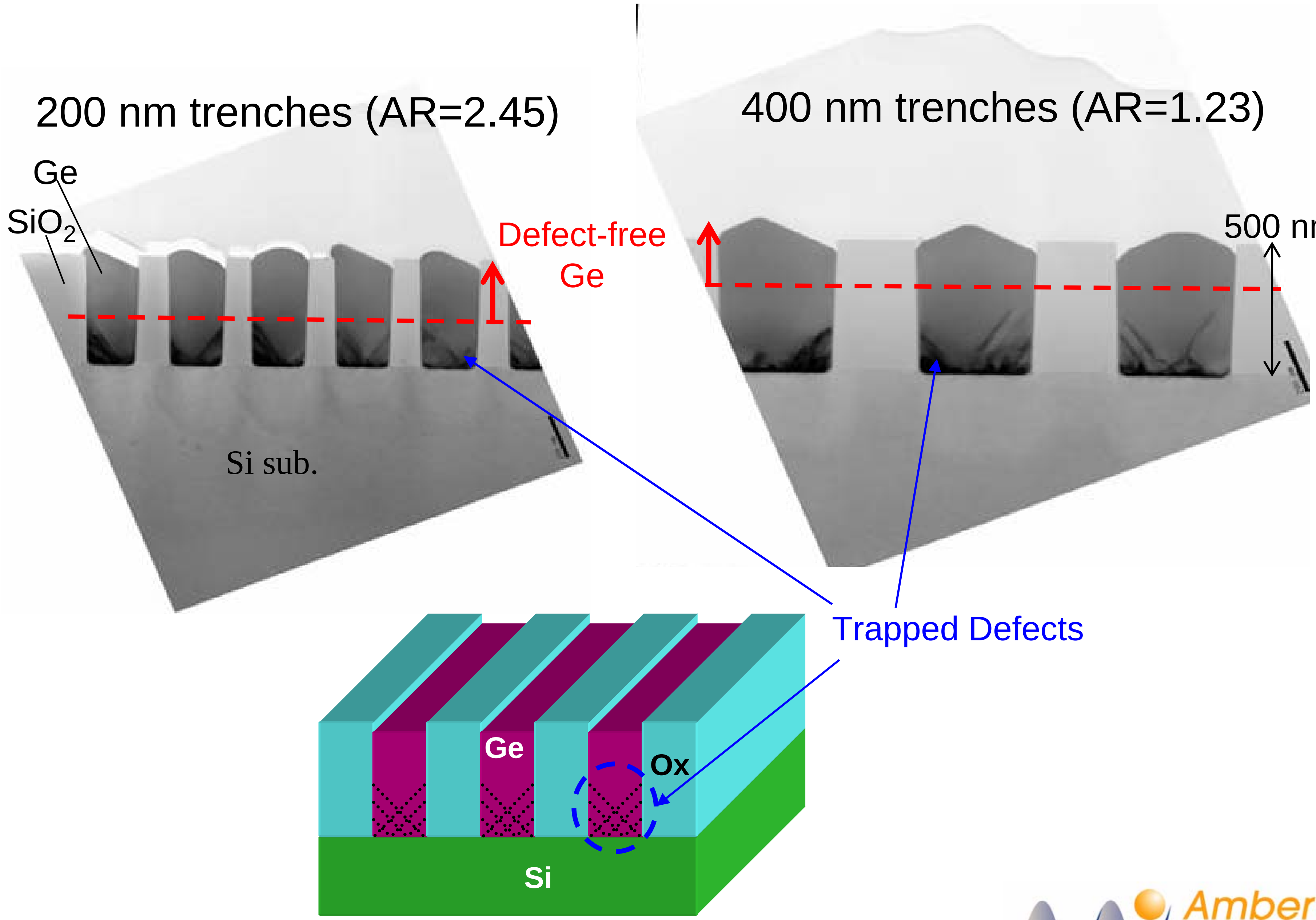
Growth Conditions

- Reactor:
  - 8” ASM Epsilon E2000 (RTCVD)
- In-situ bake:
  - 870°C for 1 min in H_2
- Growth
  - Two step in $GeH_4 + H_2$
    - ~55 nm buffer at 400°C
    - ~400 nm at 600°C
- Pressure
  - Fixed at 80 Torr

ASM growth chamber



XTEM results



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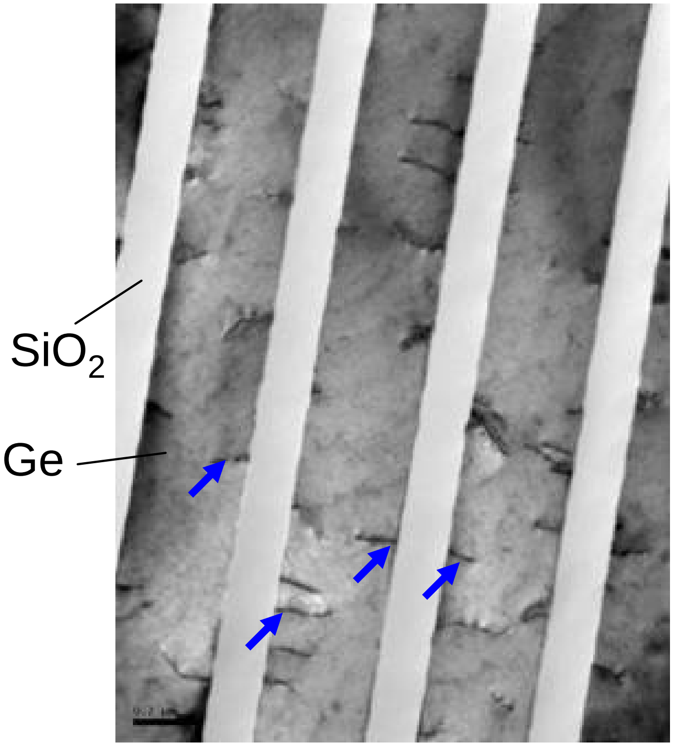
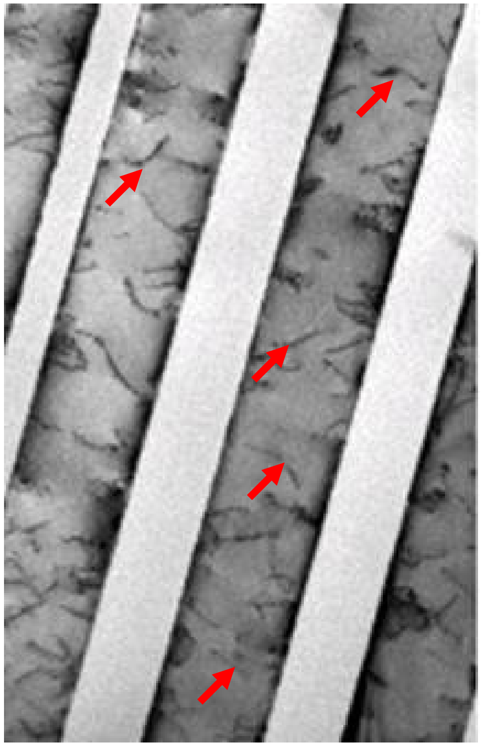
PVTEM results

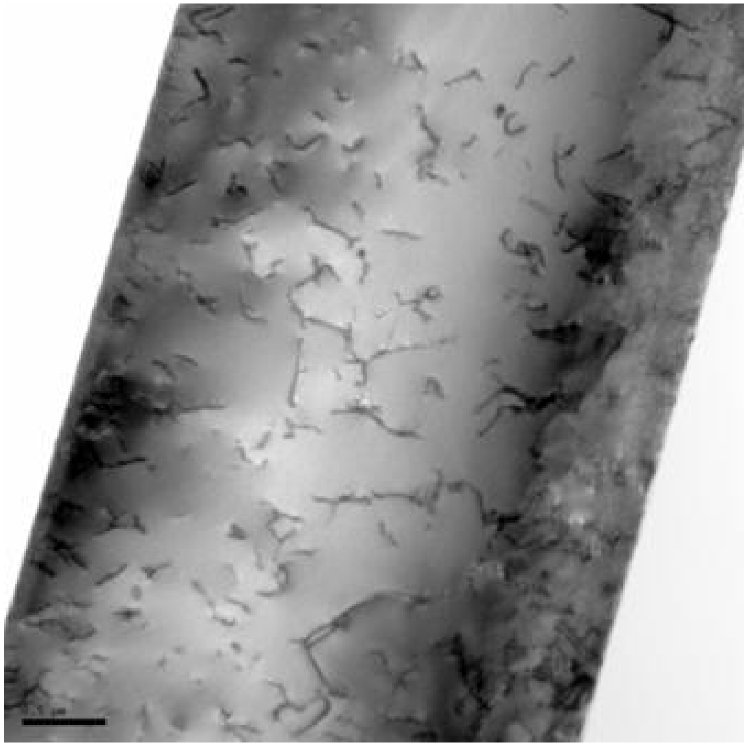
360 nm trenches
(AR= 1.36)



700 nm trenches
(AR= 0.7)



2.55 µm trenches



- AR>1;Most dislocations trapped by the oxide sidewall (↗)
- AR<1;Some dislocations terminate at the Ge surface (↗)

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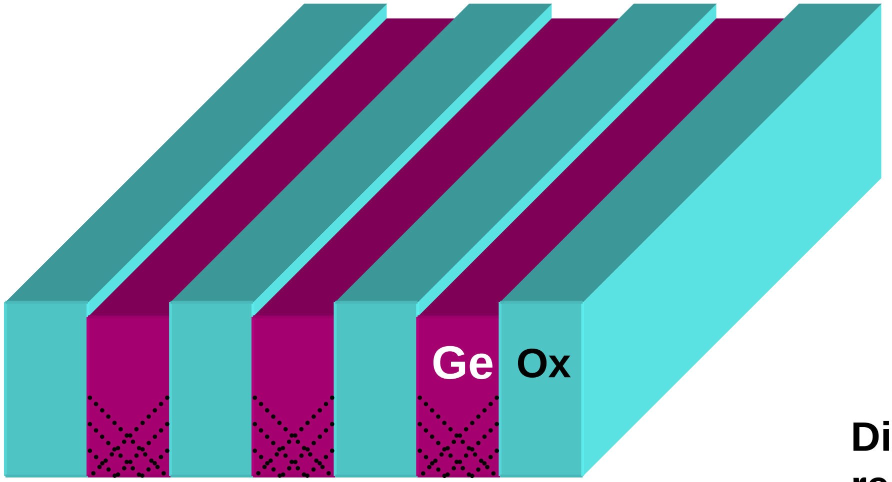
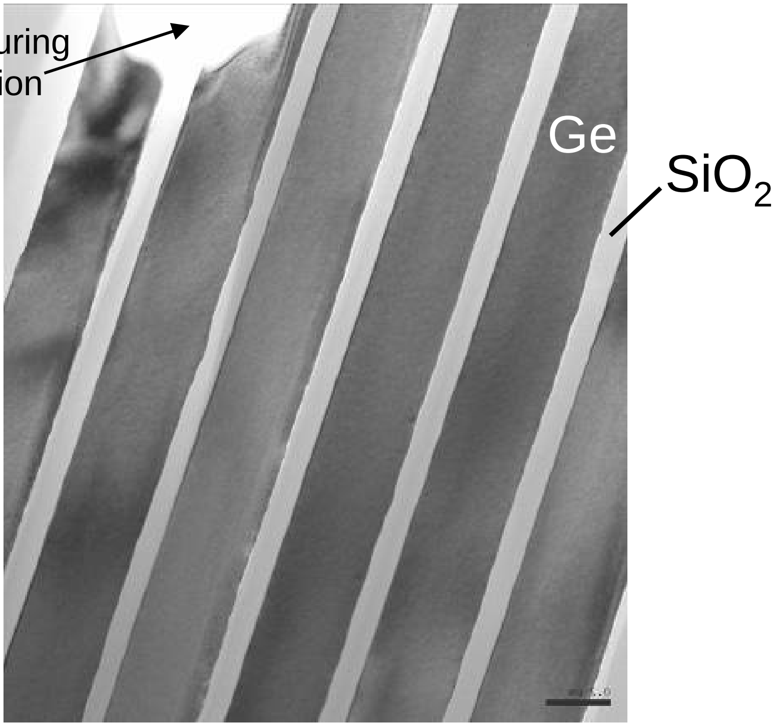
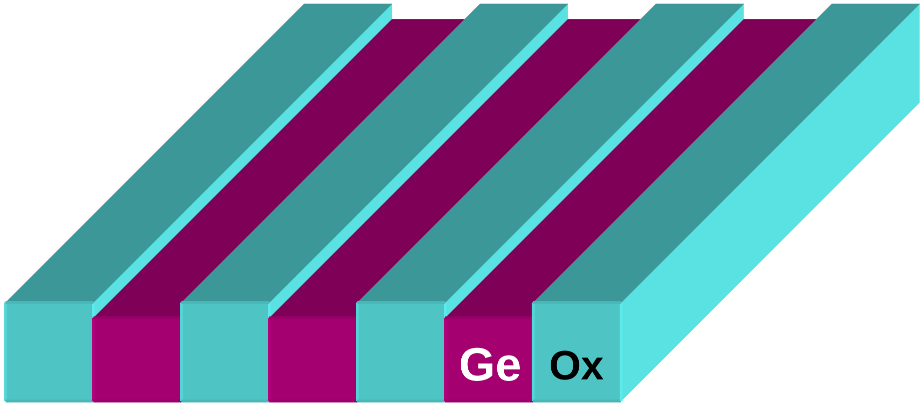
Dislocation-free top layer of Ge after trapping



290 nm wide trenches

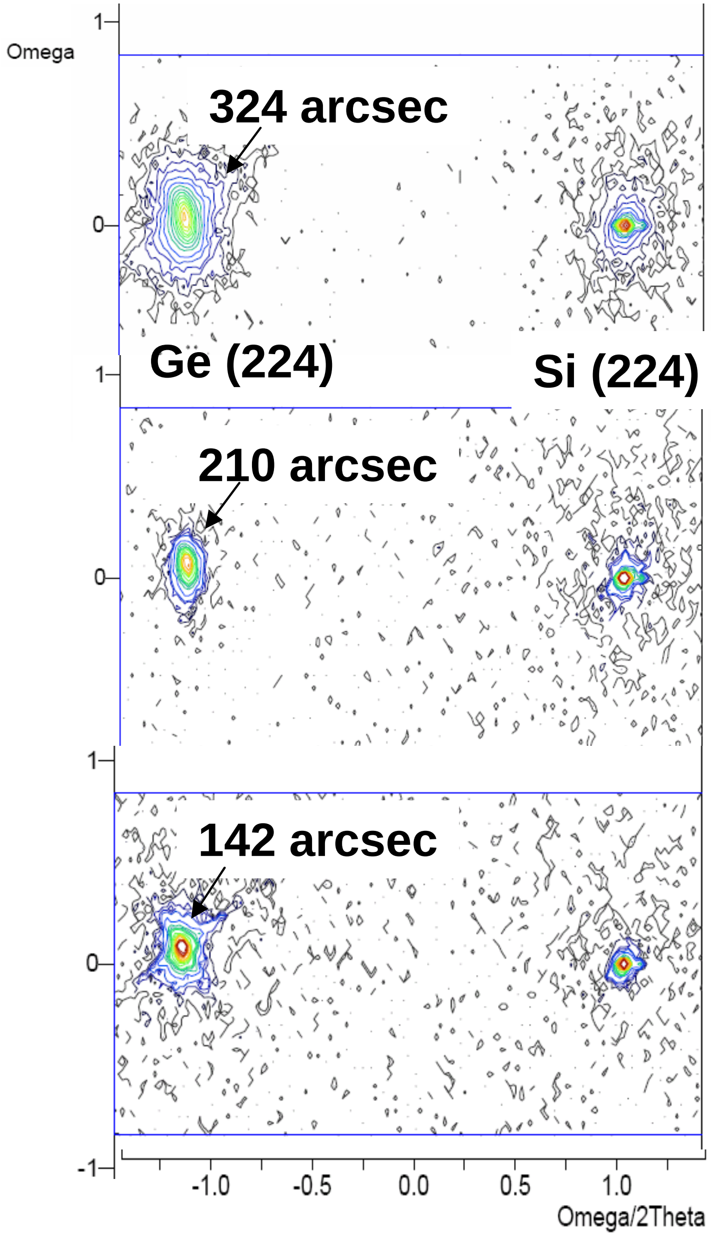
Area removed during sample preparation





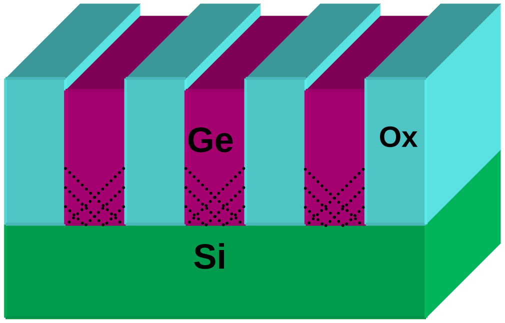
Dislocation-trapping region removed in TEM sample prep.

XRD reciprocal space map

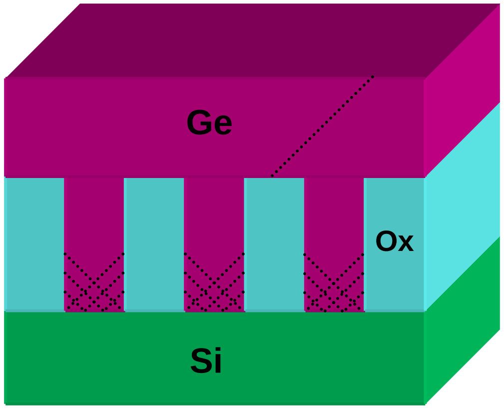


Blanket

180nm trenches 1:1 pitch



Coalesced

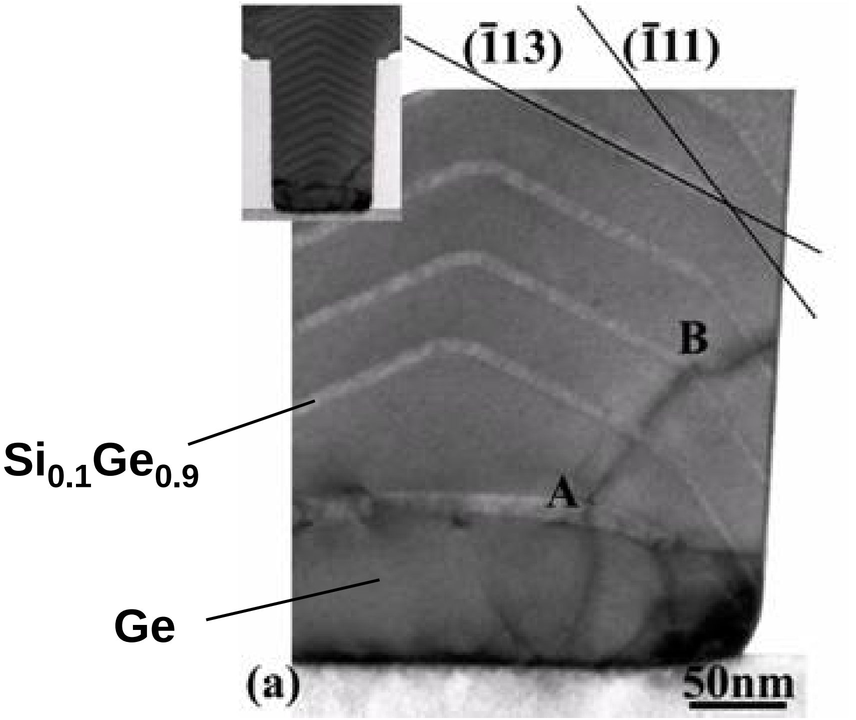


Ge is fully relaxed in each case

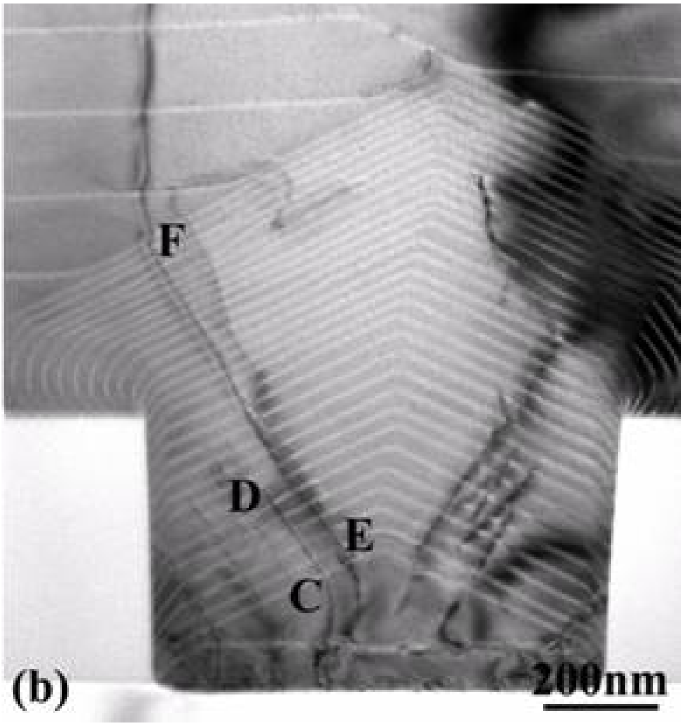
Defect reduction mechanism in Ge ART

Explore using SiGe marker layers during growth

360 nm trenches (AR= 1.36)



700 nm trenches (AR= 0.7)



- Threading dislocations (TDs) follow approximately the local facet normal direction during growth
- Very different behavior than would be expected if simply generated by mismatch driven expansion of half-loops

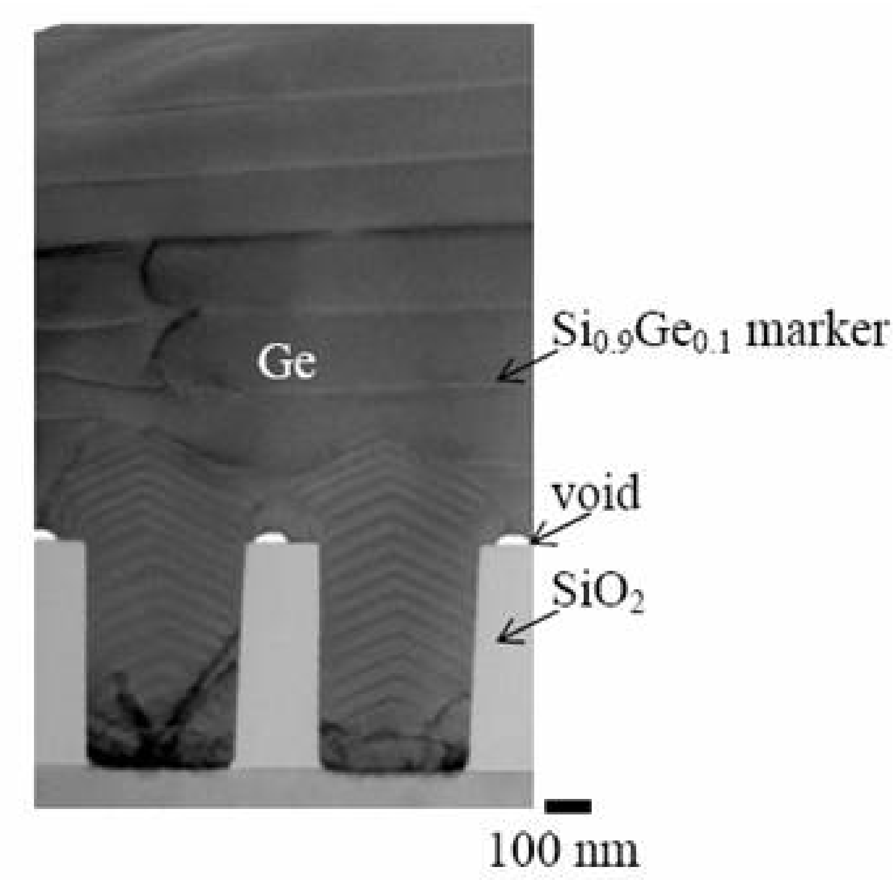
Two categories of dislocations[1]

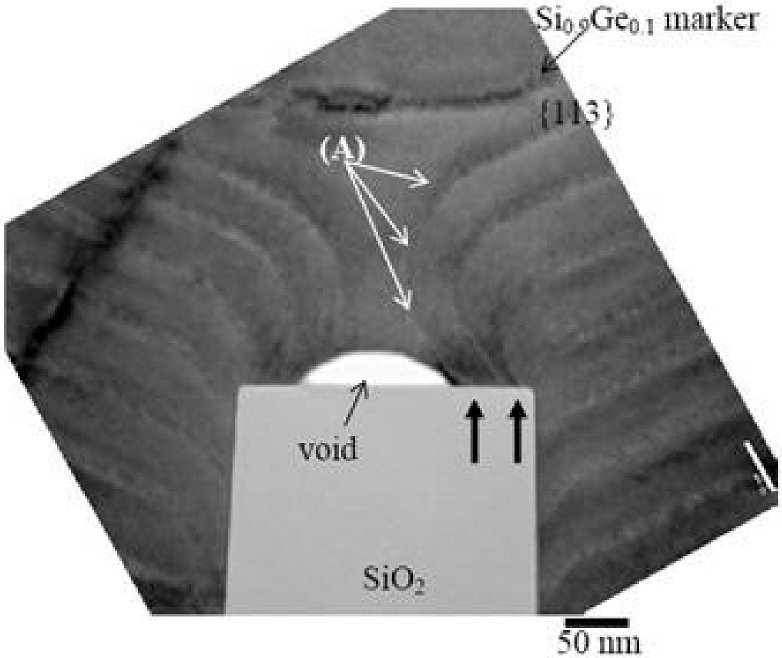
- Growth dislocation
  - Connected with the growth front and proceed with it during growth
  - Line direction determined by Burgers vector and crystal growth direction, generally approximately normal to the local growth face
- Post-growth dislocation
  - Generated behind the growth front during or after growth, e.g. through glide

- ***TD segments exhibit "growth dislocation" behavior: following facet normal direction***
- ***Facets plays crucial role in ART process, effectively guiding dislocations away from trench center***

[1] H. Klapper, Mater. Chem. Phys. 66, 101 (2000)

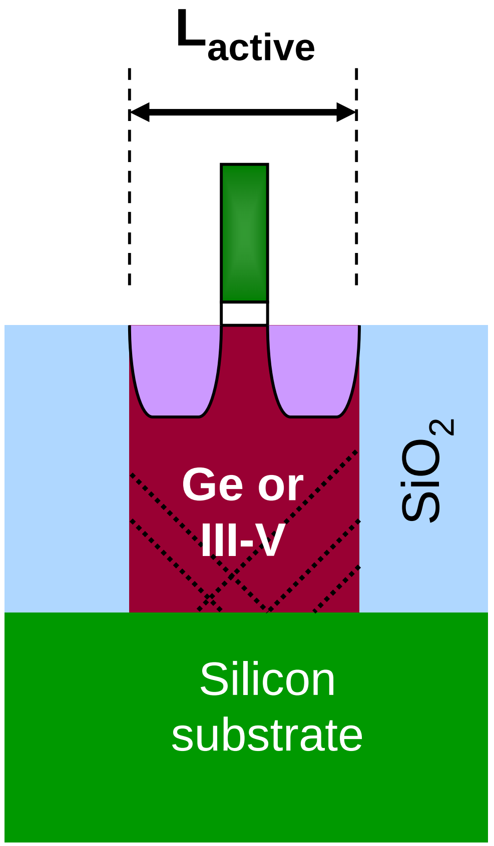
Coalescence of Ge over the sidewall

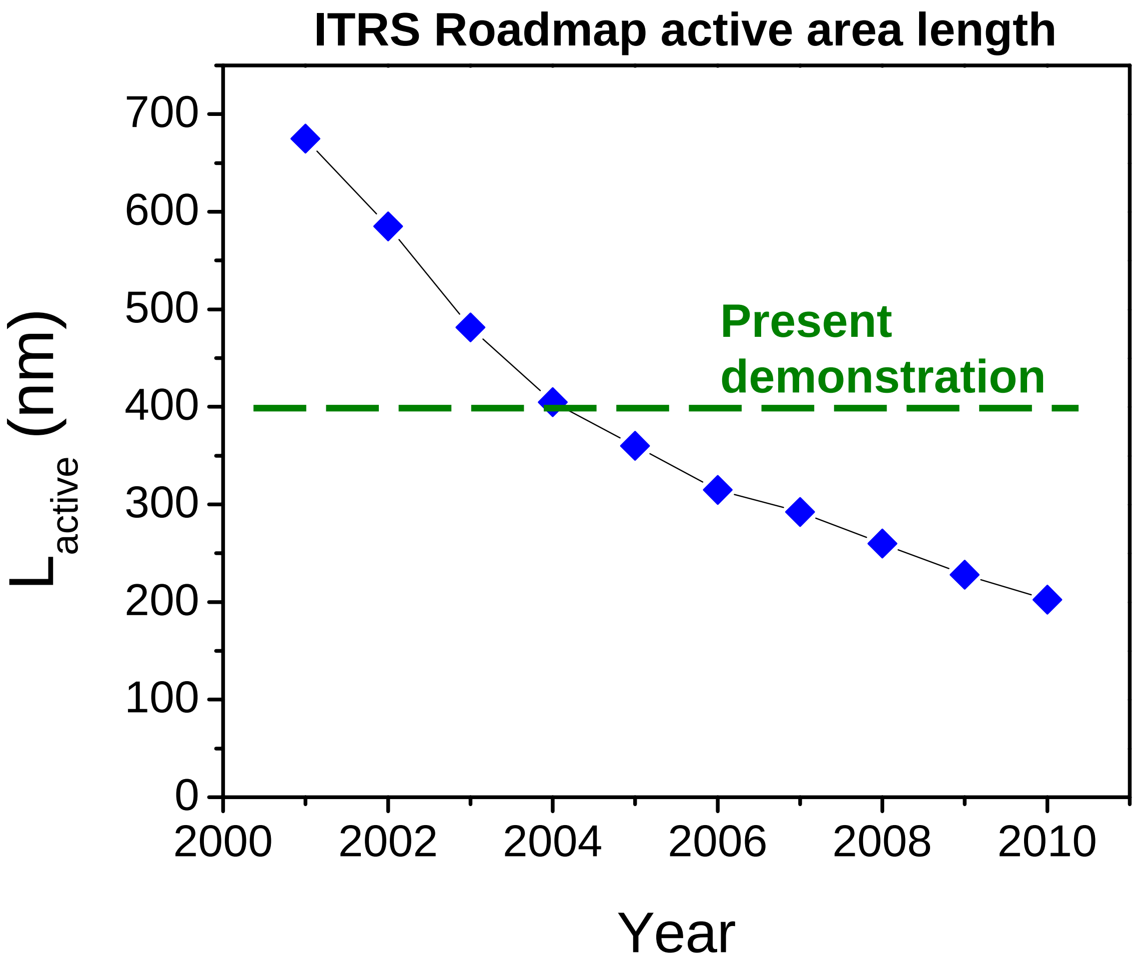




- Formation of voids and new dislocations observed upon coalescence
- {311} facets dominant before coalescence. (001) growth starts at the valley where two Ge growth fronts meet, which quickly fill up due to higher growth rate of (001).
- With increasing oxide width, coalescence and initiation of (001) growth occur more slowly.

Potential application: Alternative channel MOS





- Single ART region may serve as active area for individual transistor
- Areas for further study:
  - - Planarization of ART regions
  - - ART for III-V materials

Summary

- Dislocation trapping and defect-free Ge regions demonstrated in trenches of arbitrary length
- Dislocations follow along the facet normal direction, exhibiting growth dislocation behavior
- Void formation and new dislocation formation seen upon coalescence of individual ART regions
- Even without coalescence, regions of sufficient size for some device applications are achieved

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