Alloyed junction Ge Esaki diodes on Si substrates realised by aspect ratio trapping technique

D. Pawlik, S. Sieg, S.K. Kurinec, S.L. Rommel, Z. Cheng, J.-S. Park, J. Hydrick and A. Lochtefeld

A Ge Esaki diode is demonstrated on Si atop a coalesced epitaxial layer of Ge grown through narrow openings in SiO_2 that are used to trap threading dislocations from the lattice mismatch. Spin-on doping was used to form the n-type junction and a controlled alloyed reaction of Al and Ge forms the p-type junction. At an alloy temperature of 580°C for 1 s, the Ge-on-Si diodes were found to have a peak-to-valley current ratio of 1.1 with a peak current density of 4.1 kA/cm^2.

Introduction: Esaki diodes on a Si platform have been sought as a potential approach for building novel architectures such as tunnelling static radom access memory (TSRAM) circuits [1]. Recently several groups have pursued Esaki diodes in tunnelling transistors to obtain sub-threshold slopes as low as 13 mV/dec, a value far below the theoretical limits of conventional MOSFETs [2]. The best reports of Si-based Esaki diodes on Si have used molecular beam epitaxial growth of Si/SiGe to fabricate a vertical device structure [3–5]; these devices have been integrated with Si CMOS [6] to realise TSRAM [7]. However, the vertical nature of these structures would be challenging to gate for tunnel junction transistors [8]. Qin *et al.* have shown that heteroepitaxy of a compound semiconductor on Si will be critical to obtain high drive currents [2]. The challenge to achieve this structure lies in controlling the dislocations resulting from lattice mismatches to the host substrate.

Integration of Ge and III-V compound semiconductors on large and low-cost Si wafers have been pursued for decades. This would enable the addition of new functionality to the Si CMOS ICs and make III-V films and devices more economical. The key challenges of Ge and III-V integration onto Si substrate are thermal expansion coefficient mismatch between the two materials and the large lattice mismatch (~4% for Ge or GaAs on Si), resulting in a high density of threading dislocations. Many reports of Ge or compound semiconductors on Si rely on thick epitaxial buffers and/or high temperature anneals to mitigate defects. However, such approaches may not be easily integrable with Si-based CMOS manufacturing.

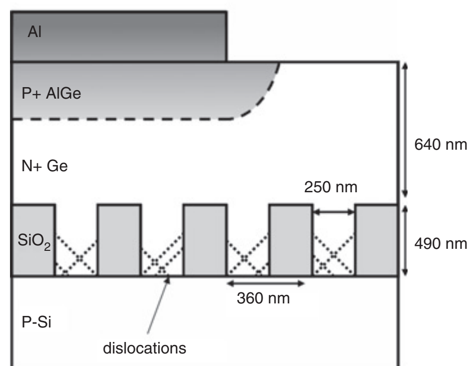

Fig. 1 *Schematic diagrams of Ge on Si Esaki diode via aspect ratio trapping epitaxy technique*

Recently, the thermal and lattice mismatch issues have been addressed by a novel technique known as aspect ratio trapping (ART) epitaxy technology, which involves a new defect reduction mechanism. Epitaxial layers of Ge [9] and III-V [10] materials are selectively grown on sub-micron wide trenches, trapping threading dislocations between the vertical dielectric sidewalls. It has been demonstrated that the dislocations for Ge and GaAs on Si can be substantially eliminated with only a few hundred nanometres of epitaxial growth [10], and without high temperature anneals. In this study, the authors use ART to grow Ge selectively on Si substrate in SiO_2-trenches and over the trenches. The Ge layer coalesces over the SiO_2 trenches, and is planarised via chemical mechanical polishing (CMP) forming a virtual Ge substrate. This material integration technique has also been shown viable for other semiconductors. In this Letter, we demonstrate a Ge on Si Esaki diode.

Experimental setup: In this study, 490 nm-thick and 250 nm-wide thermally grown oxide trench patterns (360 nm pitch) on p-type Si(001) substrates were used for Ge growth, illustrated schematically in Fig. 1, as previously described [9]. A Ge epitaxial layer was grown using reduced-pressure chemical vapour deposition and it was coalesced over the oxide trenches with a thickness of 825 nm above the oxide, which exhibits a rough surface. Coalescence defects, such as dislocations, are observed in the Ge layer when the Ge films coalesced, which will be reported elsewhere. It was then planarised on an IPEC 472 CMP to achieve a smooth 640 nm-thick Ge film above the oxide trenches. The CMP slurry was diluted Nalco 2360 (70 nm colloidal silica) slurry, with bleach added to enhance the Ge removal rate.

The device fabrication approach used in this study was adopted from Zhao *et al.* [11]. The present approach differs in two minor ways. First, this study used a lower n-type doping concentration of 5×10^{20} cm^{-3} rather than 1×10^{21} cm^{-3}. Secondly, the Zhao study utilised evaporated Al rather than sputter deposited Al: 2% Si in the present study. It was theorised that the addition of 2% Si may act to slow the reaction rate between Al and Ge, resulting in a more abrupt alloy junction.

The substrates were coated with Emulsitone 5×10^{20} cm^{-3} phosphorosilica spin-on-glass (SOG), and heat treated at 800°C for 5 min under an N_2 ambient in an AG Associates Heat Pulse 610 Rapid Thermal Annealing (RTA) furnace. This step served to introduce a degenerate level of n-type doping into the Ge. The SOG was removed in a 10:1 DI water to HF bath for 25 s. A lift-off technique was used to define dots of a 140 nm-thick Al: 2% Si, film deposited via DC sputtering. Alloying of the p-type junction was performed via a spike RTA at 480–620°C at a target time of 1 s in an N_2 ambient. A ramp rate of 150°C/s was used. In practice, the chamber temperature was in the vicinity of the target termperature for 3 s, with some run to run variability. The fabrication procedure was applied to a substrate with coalesced Ge on Si. Fig. 1 shows a schematic diagram of Ge on Si Esaki diodes.

Results: For all process conditions, negative differential resistance or inflections were observed. Fig. 2 shows the dependence of the current voltage (*I-V*) characteristics on the alloy temperature. *I-V* characteristics of 30 μm diameter diodes (anode) were measured using topside features of over 100× the area as the cathode held at ground. In general a few trends were observed. First, elevating the anneal temperatures resulted in an increase in current density. An optimal fabrication window was found for a phosphorus diffusion at 825°C, 5 min. A maximum peak-to-valley current ratio (PVCR) of 1.1 with a current density of 4.1 kA/cm^2 was observed for an alloy tempearture of 580°C, for 1 s. A 1.1 PVCR was also observed at 620°C, 1 s.

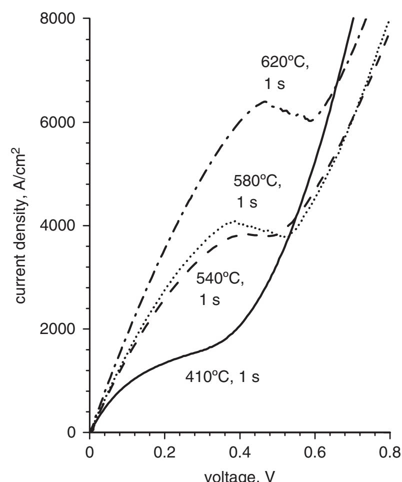

Fig. 2 *Current-voltage charateristics of 30 μm diameter ART Ge on Si Esaki diodes*

ART lines are 250 nm wide with pitch of 360 nm. Listed temperatures refer to alloy temperature which was held constant for nominal time 1 s

These results experimentally show a similar trend to those of Zhao *et al.* [11] with lower peak-to-valley ratios. It should be noted that the overall current density in the Zhao study of 15 kA/cm^2 is roughly twice the present reported value of 6 kA/cm^2 for a comparable anneal of 600°C, 1 s. This is attributed to a narrow depletion width in the Zhao study owing to the higher n-type doping levels. Based on recent

publications of P-diffusion in Si, the we estimate the junction depth for these conditions to be 300 nm [12].

For the Ge system, we believe that the Esaki diode performance can be greatly improved by exploring alternative doping schemes. It should be noted that the highest reported PVCR for Ge Esaki tunnel diodes is about 10 [13]. Davis and Gibbons further point out that Al alloying typically resulted in lower PVCR values compared to other approaches as Al consumes Ge during alloying at a much faster rate compared to Sn or In [13, 14]. Chynoweth *et al.* also indicated that alloying Al in Ge results in backward diode performance [15]. The Esaki diode performance could be further improved by optimising the aspect ratio trapping (ART) epitaxy process to reduce the coalescence defects observed on the coalesced Ge layer, which is another focus of our ongoing research. Furthermore, we predict that it will be possible to realise a III-V on an Si Esaki diode using similar techniques, which is expected to have substantially higher performance than either Si or Ge Esaki diodes.

Conclusion: We have demonstrated Ge Esaki diodes on a Si substrate with a peak-to-valley ratio of 1.1. This result suggests the high quality of Ge epi grown on trench-patterned Si substrate via aspect ratio trapping (ART) defect-trapping technique. It demonstrates a viable technique for the integration of Ge and III-V materials on Si for devices such as resonant tunnelling diodes, HEMTs and MOSFETs. Further device fabrication on III-V material on Si substrate is under development.

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