

# Preparation of Novel SiGe-Free Strained Si on Insulator Substrates

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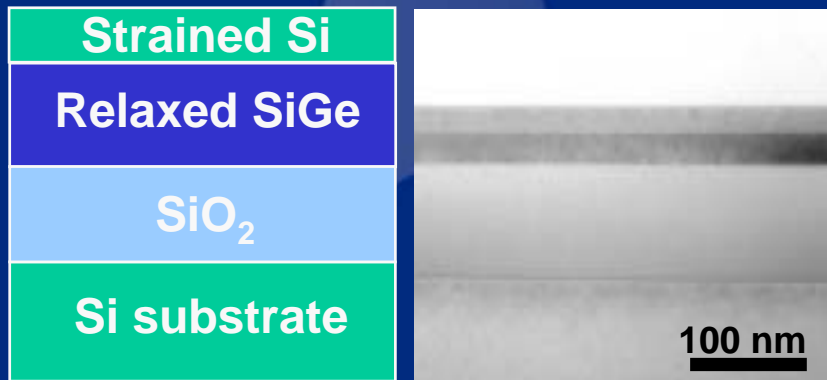
AmberWave Systems Corp., Salem, NH

October 10, 2002

- Strained Si on insulator technology
- Structure fabrication and characterization
  - Cross-section TEM
  - AFM surface roughness
  - Wafer bow film stress
  - Raman spectroscopy strain measurement
- Thermal stability
- Summary

## SiGe On Insulator

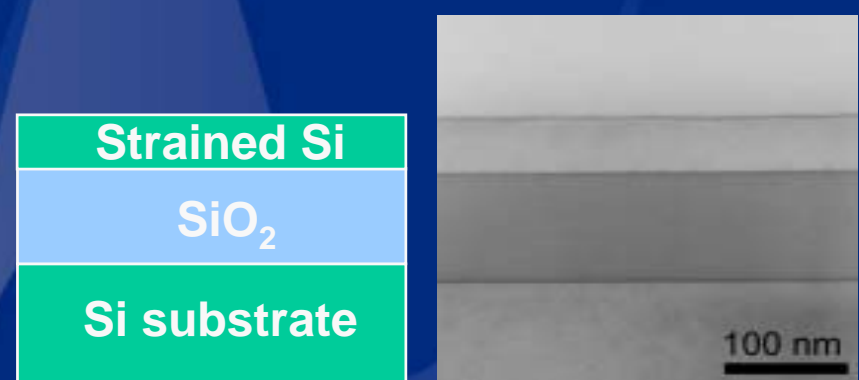
XTEM



- Combines strained Si and SOI benefits
- SiGe is strain-inducing template
- Difficult to achieve very thin structures?
- SiGe introduces process integration issues

## Strained Si On Insulator

XTEM



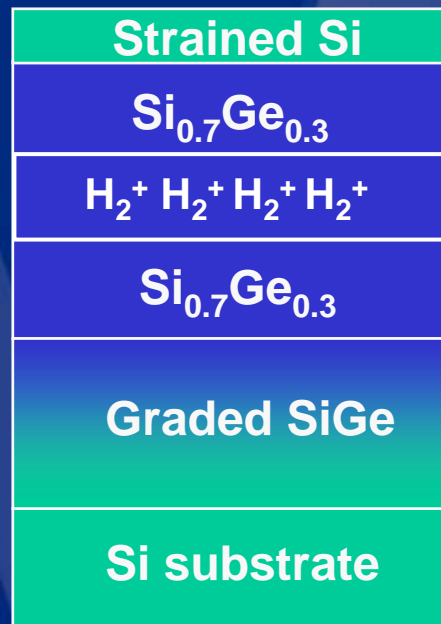
- Combines strained Si and SOI benefits
- SiGe-free structure
- Strained Si layer defined epitaxially
- Capable of very thin structures <300Å

# Strained Si on Insulator Wafer Fabrication #1

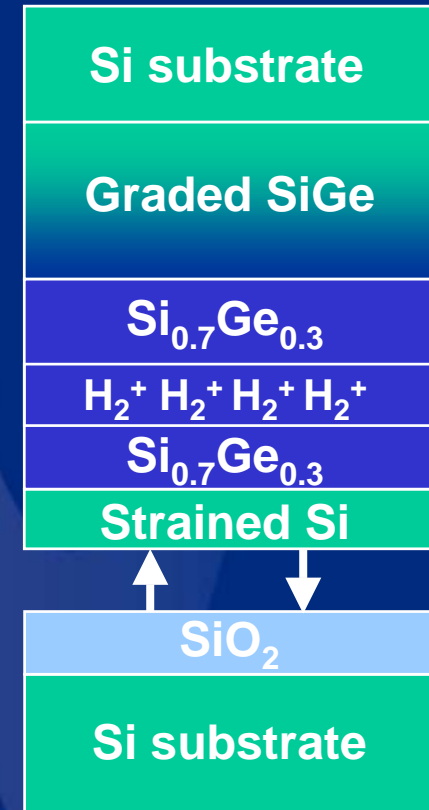
## Starting Wafer



## H<sub>2</sub><sup>+</sup> Implant

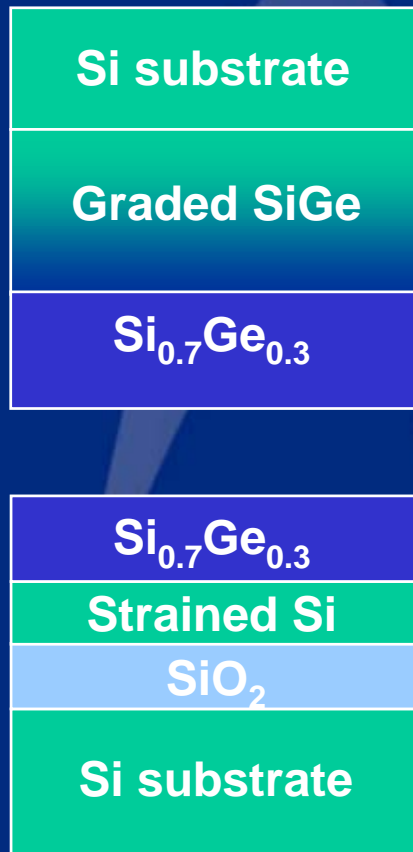


## Wafer Bond

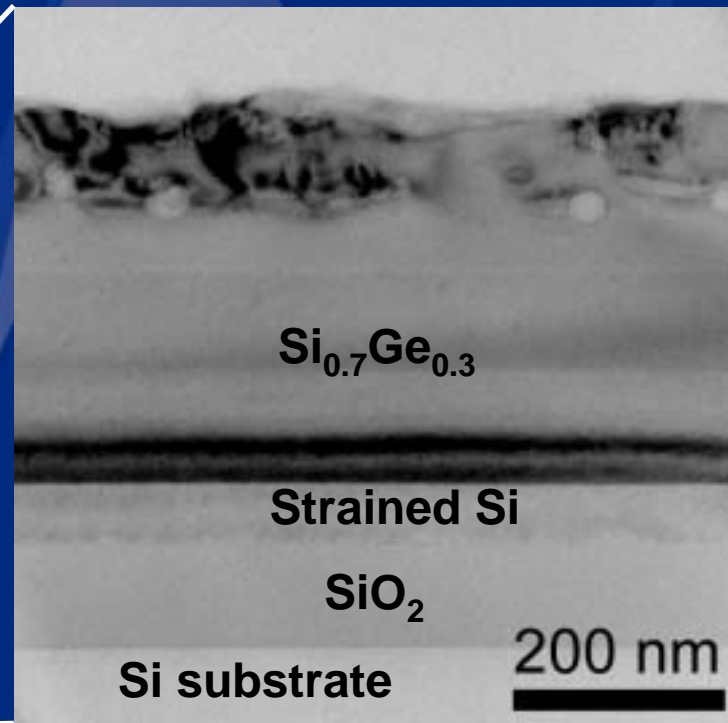


Starting material quality critical to process

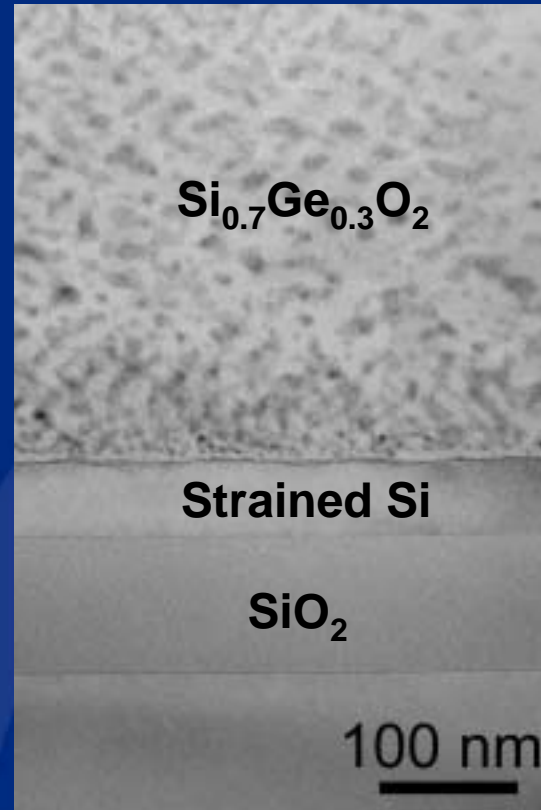
## Anneal



XTEM Image



XTEM Image

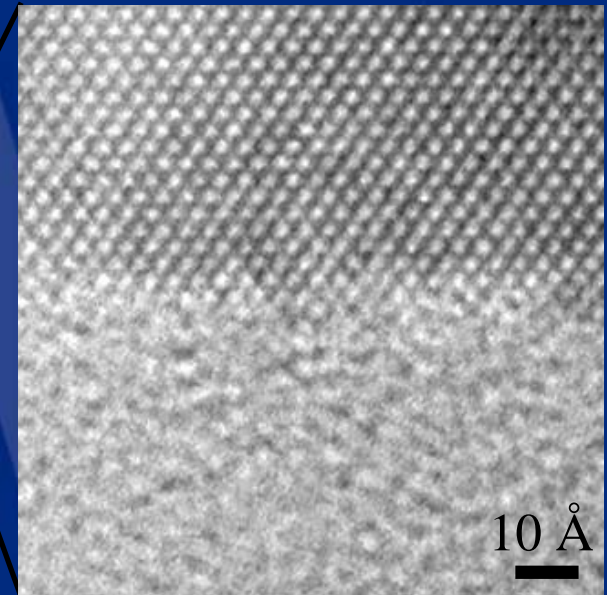
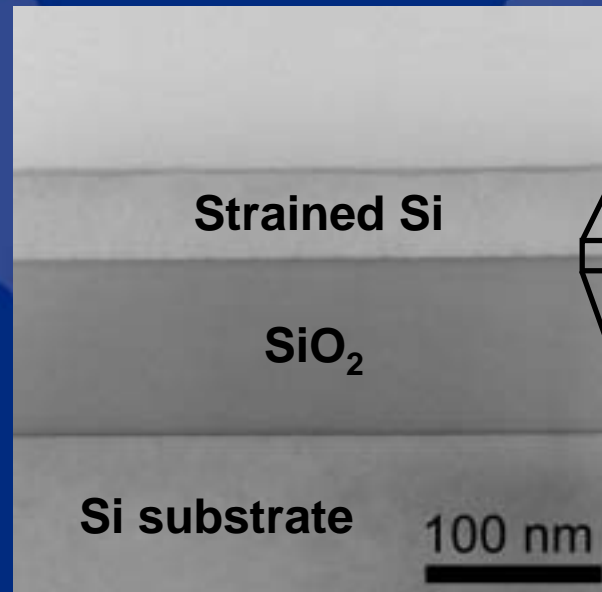


Low temperature steam oxidation SiGe removal

# SiGe-free strained Si on insulator

XTEM Image

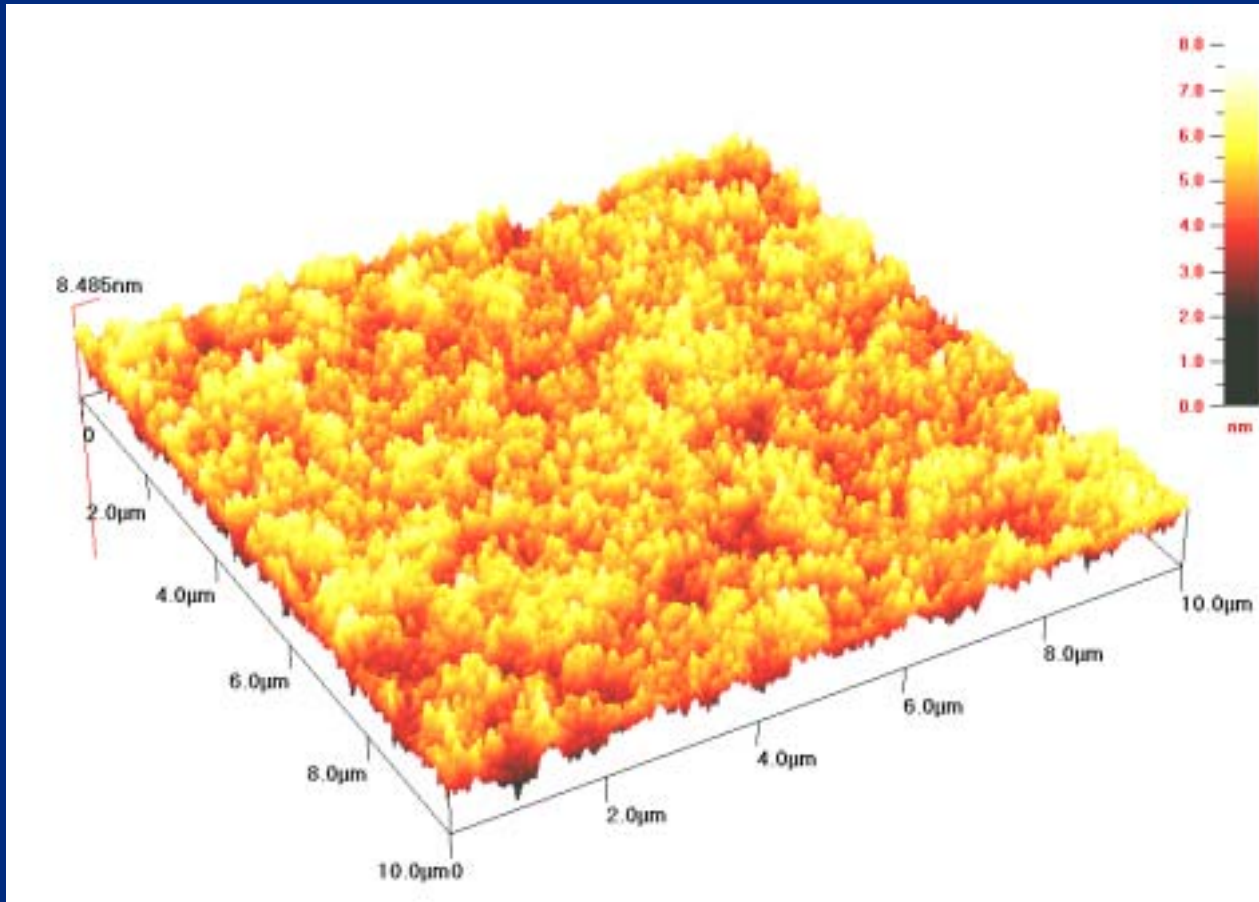
HRTEM Image



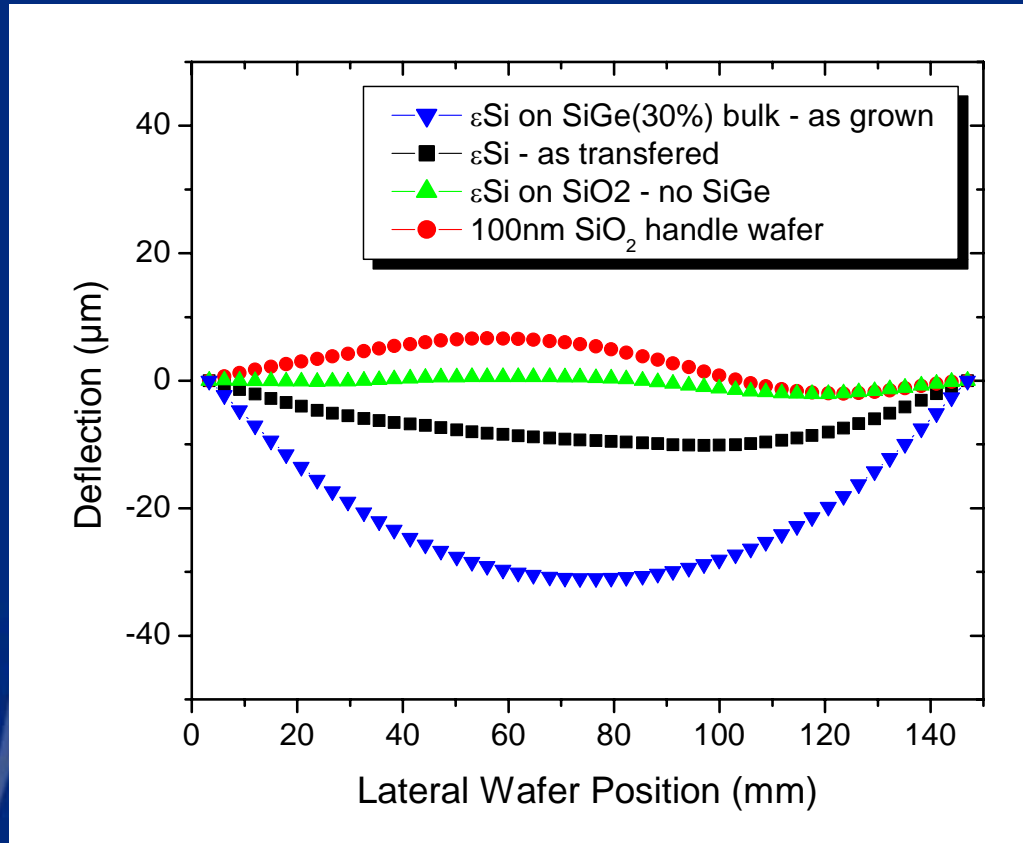
49 nm Strained Si on SiO<sub>2</sub>

Ultimate SSOI solution achieved!

# Strained Si on Insulator AFM

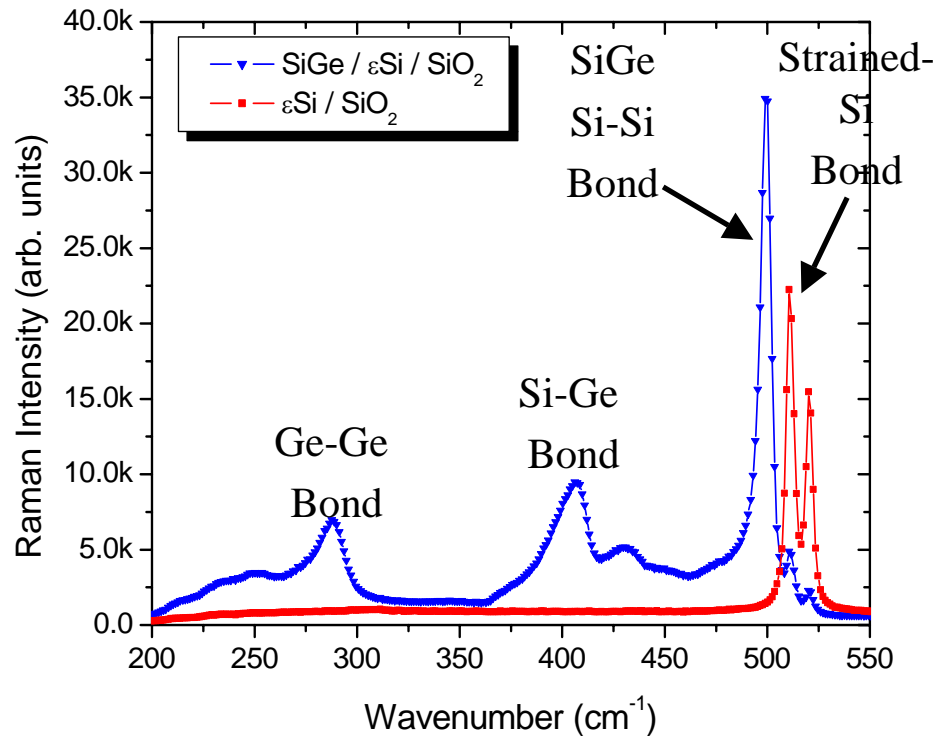


10x10 μm scan  
Post 50:1 HF  
RMS = 9.5Å  
 $R_a = 7.6\text{Å}$



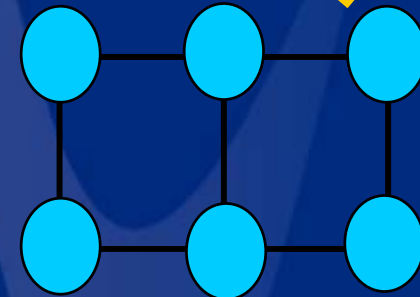
Wafer bow caused  
by film stress  
-lithography issues

Wafer bow comparable to bulk SiO<sub>2</sub> handle wafers



Incident  
514 nm laser

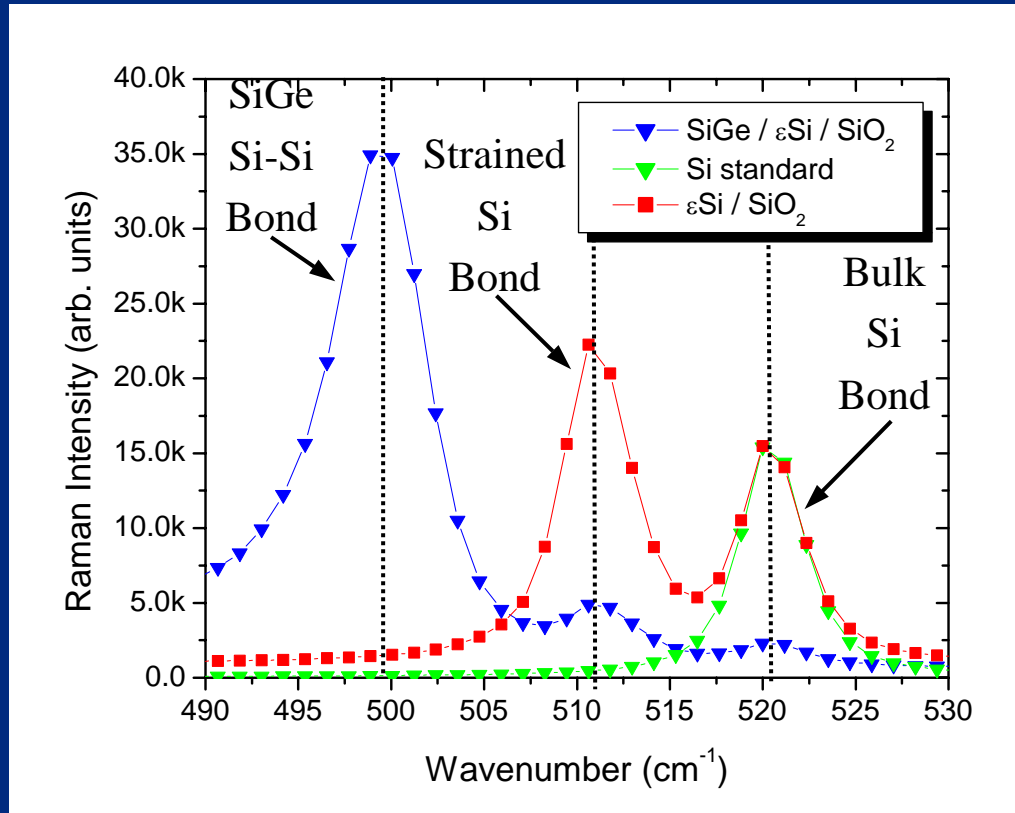
Scattered light



Light interaction with lattice phonons causes a frequency shift

Complete SiGe removal by oxidation

# Strained Si on Insulator Raman Spectroscopy



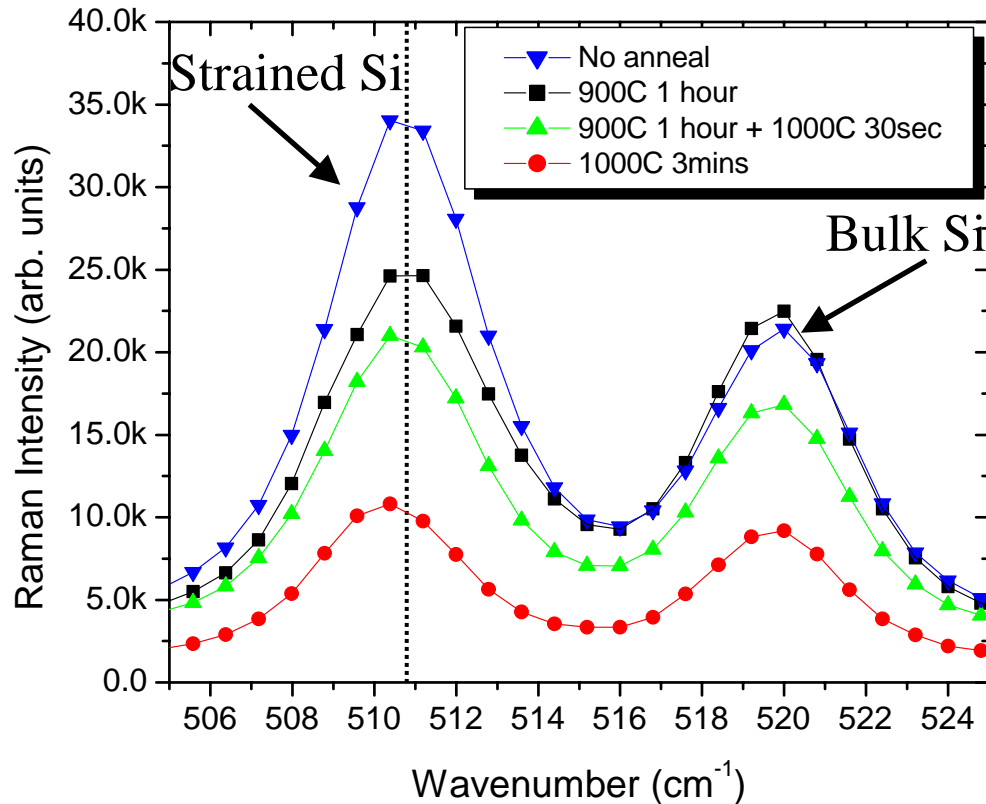
$$\epsilon = 0.123(\omega_{\text{Strained Si}} - \omega_{\text{bulk Si}})$$

$$\omega_{\text{Strained Si}} = 510.9 \text{ cm}^{-1}$$

$$\omega_{\text{bulk Si}} = 520.2 \text{ cm}^{-1}$$

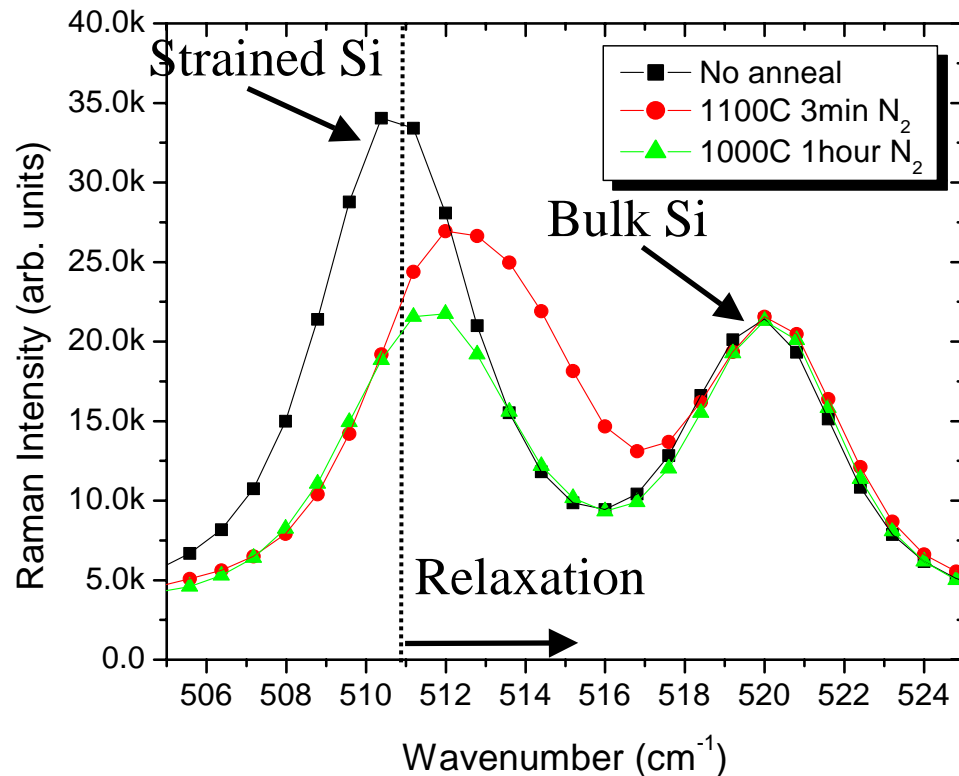
$$\epsilon = -1.14\%$$

> 1% tensile strain maintained without SiGe!



- Strained Si peak remains at 510.9 cm<sup>-1</sup>
- No peak shift = no strain loss!

>1% strain unaffected by normal CMOS thermal budgets



	Si Strain Level (%)
No anneal	1.14
1000°C 1 hr	1.04
1100°C 3 min	0.88

Extreme thermal budgets cause slight film relaxation

- **Ideal strained Si on insulator structure achieved**
- **Finished structure is SiGe-free**
- **Tensile Si strains of greater than 1% demonstrated**
- **Strained Si thermal budget limitations alleviated**

## Acknowledgements

We would like to thank D. Robbins and M. Saker of QinetiQ, U.K. for Raman measurements. Helpful discussions with G. Taraschi of MIT are acknowledged.