

Inversion-type enhancement-mode InP MOSFETs with ALD Al₂O₃, HfO₂ and HfAlO nanolaminates as high-k gate dielectrics

Y.Q. Wu¹, Y. Xuan¹, P.D. Ye^{1,*}, Z. Cheng², A. Lochtefeld²

¹ School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906

² AmberWave Systems Corp., 13 Garabedian Drive, Salem, NH 03079

* Tel: 765-494-7611, Fax: 765-494-0676, E-mail: yep@purdue.edu

With recent announcements from Intel and IBM regarding implementation of atomic-layer-deposition (ALD) high-k gate dielectrics and metal gates in high-volume manufacturing for upcoming complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs), the potential for novel channel materials for future CMOS ICs is growing. By eliminating SiO₂ as the gate dielectric for the channel surface, a key advantage of Si over compound semiconductors is minimized; there is a growing hope that the ALD high-k dielectrics developed for Si may also be applicable to compound semiconductors. Although high-performance depletion-mode (D-mode) GaAs MOSFETs have been demonstrated by various research groups, the reported inversion-type enhancement-mode (E-mode) GaAs MOSFETs suffer from relatively low drain currents.¹⁻³

In this paper, we report on fabricating inversion-type E-mode n-channel InP MOSFETs using ALD Al₂O₃, HfO₂, and HfAlO nanolaminates as high-k gate dielectrics and demonstrating more than a factor of 1000 increase in maximum drain current, compared to inversion-type E-mode GaAs MOSFETs.¹⁻³ InP is widely believed to be a more forgiving material with respect to Fermi level pinning and has a higher electron saturation velocity (2×10^7 cm/s) as well. Detailed Monte-Carlo simulations of deeply scaled n-MOS devices indicate that an InP channel could enable high-field transconductance ~60% higher than either Si, Ge, or GaAs at equivalent channel length⁴. Fig. 1 and Fig. 2 show the schematic cross section of the device structure and the process flow. Table 1 summarizes the device performance of the same gate length devices with different gate dielectrics in terms of maximum drain current, peak transconductance, and drain current drifts. ALD Al₂O₃ shows better interface properties than HfAlO and HfO₂, though its k value is about half of HfO₂ and HfAlO. Our detailed analysis on device characteristics in this abstract is focused on ALD Al₂O₃ only due to the limited space. A well-behaved I-V characteristic of an E-mode InP NMOSFET is demonstrated in Fig. 3 with maximum drain current of 78 mA/mm and Al₂O₃ thickness of 8 nm. Fig. 4 shows the effective gate length (L_{eff}) and series resistance (R_{SD}) extracted by plotting channel resistance R_{Ch} vs. mask gate length L_{Mask} which is important to determine the intrinsic device performance and accurately extract the effective mobility. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics is calculated by subtracting R_{SD} and using L_{eff} instead of L_{Mask} and is compared with the extrinsic counterparts as shown in Fig. 5. The threshold voltage is determined to be 0.5 V for Al₂O₃ (8nm) and 1.3V for HfAlO (8nm), respectively. Fig. 6 shows the sub-threshold slope (S.S.) and DIBL characteristics of 280 mV/dec. and 50 mV for 8 nm Al₂O₃ devices. As shown in Fig. 7, the "split-CV" method is used and the extracted mobility has a peak value of 650 cm²/Vs around a normal electric field of 0.22 MV/cm. Fig. 8 shows a representative C-V characteristic of an Al₂O₃ (8nm)/n-InP MOS capacitor with a clear transition from accumulation to depletion for HF C-V and the inversion features for LF C-V and quasi-static C-V, which demonstrates channel inversion operation. It verifies that the conventional Fermi-level pinning phenomenon reported in the literature is overcome in this ALD high-k/InP material system with a mid-gap D_{it} of $2-3 \times 10^{12}$ /cm²-eV determined by HF - LF method. More detailed analysis on HfO₂ and HfAlO devices with different surface treatments, compared to Al₂O₃, is ongoing.

We demonstrate here the use of ALD high-k dielectrics for the fabrication of E-mode InP MOSFETs exhibiting well-behaved transistor characteristics. These results suggest new opportunities for evaluating and applying InP as a novel high-mobility channel material for future ultimate CMOS applications.

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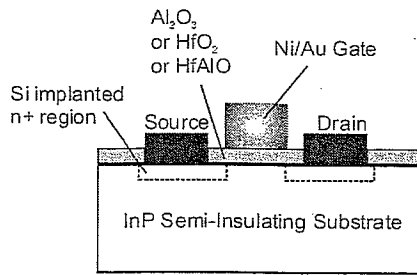


Fig. 1 Schematic view of an E-mode n-channel InP MOSFET with ALD Al_2O_3 , HfO_2 or HfAlO as gate dielectrics.

- Surface clean and pretreatment $(\text{NH}_4)_2\text{S}$
- Deposition of 30nm Al_2O_3 using ALD
- Ion Implantation (Si 35Kev, $1 \times 10^{14}/\text{cm}^2$)
- Activation using RTA 720 °C for 10sec
- For regrown oxide, etch away oxide using BHF and regrow 8nm Al_2O_3 or HfO_2 or HfAlO and PDA
- S/D region patterning and metal deposition AuGe/Ni/Au and RTA
- Gate region patterning and metal deposition Ni/Au

Fig. 2 Fabrication process flow for E-mode high-k/InP MOSFETs. 30 nm thick Al_2O_3 is used as an encapsulation layer for dopant activation process, while thin regrown Al_2O_3 , HfO_2 and HfAlO is used as high-k gate dielectrics.

$V_g=5\text{V}$ $V_d=2\text{V}$ $L_g=2\mu\text{m}$	Al_2O_3 30nm As-growth	Al_2O_3 8nm Re-growth	HfAlO 8nm Re-growth	HfO_2 8nm Re-growth
I_{ds} (mA/mm)	32	67	55	<50
g_{max} (mS/mm)	8.5	22	20	~20
I_{ds} drift percent (10^4 sec)	12%	5%	35%	~35%

Table 1 Drain current, transconductance, drain current drift vs. the same gate length InP MOSFETs with the different Al_2O_3 , HfO_2 and HfAlO as dielectrics.

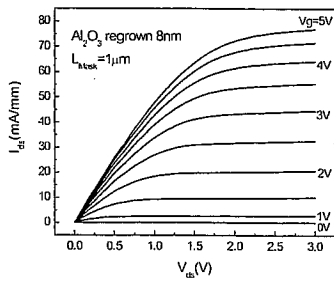


Fig. 3 Drain current vs. drain bias as a function of gate bias for 1 μm InP MOSFET with 8 nm regrown Al_2O_3 as gate dielectric.

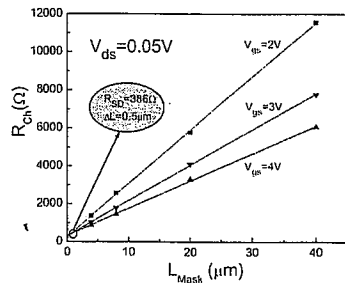


Fig. 4 Measured channel resistance vs. different mask gate length as a function of gate bias. Three dashed fitting lines are used to determine R_{SD} and ΔL . Al_2O_3 thickness is 30 nm

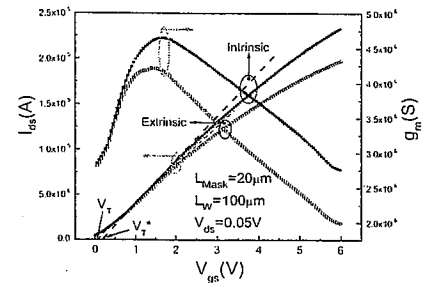


Fig. 5 Extrinsic (empty) and intrinsic (solid) drain current and transconductance versus gate bias. The dashed lines are eye-guided to determine the threshold voltage of the devices.

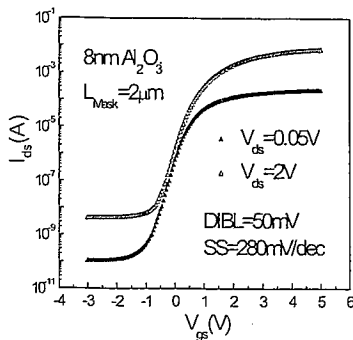


Fig. 6 Drain current versus drain bias as a function of gate bias for 2 μm InP MOSFET with 8nm Al_2O_3 oxide.

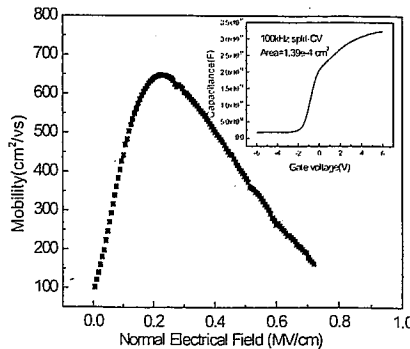


Fig. 7 Effective mobility versus normal electric field for the InP MOSFET with 30 nm Al_2O_3 as gate oxide. Inset is 100kHz split-CV measurement of the MOSFET.

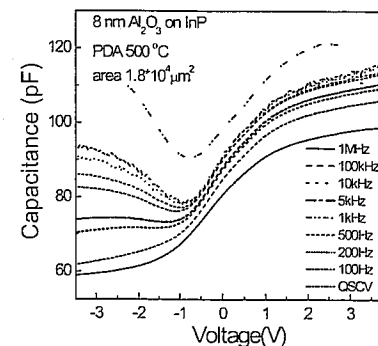


Fig. 8 C-V measurements on 8 nm Al_2O_3 /n-InP MOSCAP from quasi-static up to 1MHz.