INVERSION-TYPE ENHANCEMENT-MODE INP MOSFETS WITH ALD HIGH-K AL_2O_3 AND HFO_2 AS GATE DIELECTRICS

Y.Q. Wu [1], M. Xu [1], Y. Xuan [1], P.D. Ye [1,*], J. Li [2], Z. Cheng [2], A. Lochtefeld [2]
[1] *School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906*
[2] *AmberWave Systems Corp., 13 Garabedian Drive, Salem, NH 03079*
* *Tel: 765-494-7611, Fax: 765-494-0676, E-mail: yep@purdue.edu*

Abstract — **Enhancement-mode (E-mode) n-channel InP metal-oxide-semiconductor field-effect-transistors (MOSFETs) with 0.75 to 40 µm gate length fabricated on semi-insulating substrates and p-type doped InP epi-layers with atomic-layer-deposited (ALD) Al_2O_3 and HfO_2 as gate dielectrics are demonstrated. The ALD process on III-V compound semiconductors enables the formation of high-quality gate oxides and unpinning of Fermi-level on compound semiconductors. A 1-µm gate-length E-mode n-channel MOSFET with a HfO_2 gate oxide thickness of 10 nm shows a maximum drain current of 130 mA/mm and a trans-conductance of 40 mS/mm at the highest gate bias of 6 V.**

***Keywords** - ALD, high-k, III-V compound seminconductors, MOSFET*

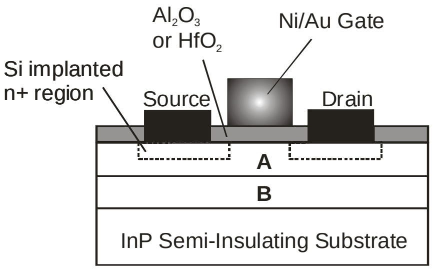
I. INTRODUCTION

Finding a suitable gate dielectric to make III-V metal-oxide-semiconductor (MOS) devices has been regarded as something of a “holy grail” in III-V compound semiconductor research community. Lacking a suitable gate insulator, practical III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) remain all but a dream for more than four decades.[1-4] Heterogeneous integration of novel dielectrics and novel channel materials has recently gained increasing attention as a necessity to further drive Si complementary metal-oxide-semiconductor (CMOS) integration, functional density, speed and power dissipation, and to extend CMOS front-end fabrication to and beyond the 22-nm node. The successful deposition of high-*k* dielectrics on Si at relatively low temperatures has raised the hope for extending the approach to III-V compound semiconductors. For the first time in history, the latest edition of the ITRS roadmap refers compound semiconductor based transistors as a “nonclassical” CMOS solution to continue long term scaling according to Moore’s law. Enormous research efforts are building up world wide again at finding ways to fabricate III-V MOSFETs using CMOS technology. [5-21]

In terms of III-V gate dielectrics, three major approaches are focused currently by industry and academia: (1) the conventional ALD high-k dielectric process with appropriate surface treatment;[18-21] (2) molecular beam expitaxy (MBE) grown Ga_2O_3 and Gd_2O_3; [5-7,9,11](3) using Si or Ge interface control layer (ICL) in between deposited high-k and III-V compound semiconductors.[4,10,12] Compared to MBE approach, ALD approach is an ex-situ, robust, and manufacturable method demonstrated by Si industry. Compared to ICL approach, it avoids the complication of C-V data interpretation and potential Si/Ge interdiffusion into III-V at high temperature process. In this paper, we demonstrate that inversion-type E-mode n-channel MOSFETs on semi-insulating InP substrates with maximum drain current of ~130 mA/mm using ALD HfO_2 as high-k gate dielectric. We also report on device performance dependence on the doping concentration of the InP channel layers. InP is a widely studied III-V compound semiconductor with a high electron saturation velocity (2×10^7cm/s). Detailed Monte-Carlo simulations of deeply scaled n-MOS devices indicate that an InP channel could enable high-field transconductance ~60% higher than either Si, Ge, or GaAs at equivalent channel length [22]. It is also believed that InP is a more forgiving material in terms of Fermi level pinning, compared to GaAs.[23-24] Compared to recently demonstrated world-record InGaAs MOSFETs, InP has wider bandgap and should not have issues related with band-to-band-tunneling, impact ionization, and low On/Off ratio.

II. SAMPLE FABRICATION

Fig. 1 shows the schematic cross section of the device structure of an ALD Al_2O_3 or HfO_2 InP MOSFET fabricated on InP semi-insulating substrate or p-type epitaxial InP layers.



Structure 1: A and B is semi-insulating substrate
Structure 2: A is InP, 300 nm thick and $1\times10^{17}/cm^3$ p-doping
B is InP, 500 nm thick and $4\times10^{17}/cm^3$ p-doping
Structure 3: A is InP, 300 nm thick and $2\times10^{17}/cm^3$ p-doping
B is InP, 500 nm thick and $1\times10^{18}/cm^3$ p-doping

Fig. 1 Schematic view of an E-mode n-channel InP MOSFET with ALD Al_2O_3 and HfO_2 as gate dielectrics.

After surface degreasing and $(NH_4)_2S$-based pretreatment, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al_2O_3 layer was deposited at a substrate temperature of 300^{o}C, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) in a carrier N_2 gas flow. Source and drain regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 140 keV through the 30 nm thick Al_2O_3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 720 ^{o}C for 10s in a nitrogen ambient. The Al_2O_3 encapsulation layer was removed by HF and Al_2O_3 or HfO_2 gate dielectrics were grown by ALD again with the thickness between 4nm to 10 nm. The source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Pt/Au and a lift-off process, followed by a RTA process at 500 ^{o}C for 30s also in a N_2 ambient. The gate electrode was defined by electron beam evaporation of Ti/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.75 µm to 40 µm and a gate width of 100 µm. Figure 2 shows the detailed fabrication process flow. [23-24]

- Surface clean and pretreatment $(NH_4)_2S$
- Deposition of 30nm Al_2O_3 using ALD
- Ion Implantation (Si 35Kev, $1\times10^{14}/cm^2$)
- Activation using RTA 720 ^{o}C for 10sec
- For regrown oxide, etch away oxide using BHF and regrow 8nm Al_2O_3 or HfO_2 and PDA
- S/D region patterning and metal deposition AuGe/Ni/Au and RTA
- Gate region patterning and metal deposition Ni/Au

Fig. 2 Fabrication process flow for E-mode high-k/InP MOSFETs. 30 nm thick Al_2O_3 is used as an encapsulation layer for dopant activation process, while thin regrown Al_2O_3 and HfO_2 is used as high-k gate dielectrics.

III. RESULTS AND DISCUSSIONS

A well-behaved I-V characteristic of an E-mode InP NMOSFET with 10 nm HfO_2 as gate dielectric is demonstrated in Fig. 3 with maximum drain current over 100 mA/mm at V_{ds}=3V and V_{gs}=4V. The device was simply fabricated on semi-insulating InP substrate (Structure 1 as shown in Figure 1). The device is off at V_{gs}=0 V without significant drain-source leakage current or substrate current due to the high bandgap of InP. In general, it is surprised to obtain 100 mA/mm level drain current on InP substrate since only a few hundreds of µm/mm drain current was observed on GaAs without ICL layer. We ascribe it to the fact that the energy separation between conduction band minimum (CBM) and charge neutrality level (CNL) for InP is 0.5 eV instead of 0.8 eV for GaAs. This makes it easier for InP to realize inversion, compared to GaAs.

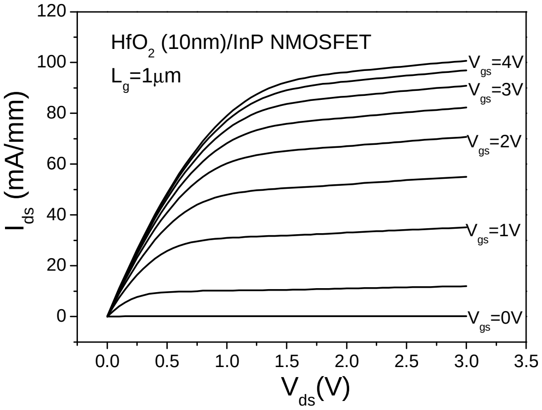


Fig. 3 Drain current vs. drain bias as a function of gate bias for 1 µm InP MOSFET with 10 nm regrown HfO_2 as gate dielectric (Structure 1).

Fig. 4 shows the transfer characteristics of Al_2O_3 and HfO_2 InP NMOSFETs. The HfO_2 device has 130 mA/mm maximum drain current versus 75 mA/mm maximum drain current for Al_2O_3 device due to the effect of "high-k". At the same gate bias, the capacitance or the surface electric field in semiconductors is larger for high-k. That's why HfO_2 MOSFET shows higher drain current though its thickness is 10 nm, 2 nm more than Al_2O_3. It is a balance between high-k value and maximum electric strength. The higher k value is, the lower the maximum electric strength. The real figure-of-merit is related with the product of high-k value and maximum electric strength.

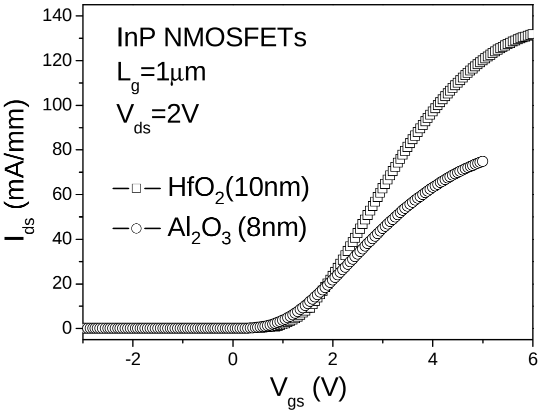


Fig.4 Measured transfer characteristics of HfO_2 and Al_2O_3 InP MOSFETs with 1µm gate length and V_{ds}=2V (Structure 1).

The transconductance of HfO_2 MOSFET is also higher than Al_2O_3 MOSFET as shown in Fig. 5. If we suppose the interface trap density D_{it} of Al_2O_3 and HfO_2 on III-V is comparable, the saturation velocity on InP should be similar. The big different in peak transconductance G_m is from the difference of gate capacitance. With similar oxide thickness and geometry, the k-value of the oxide is the most important factor.

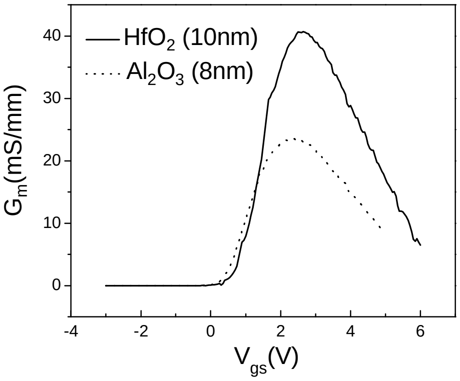


Fig. 5 Measured transconductance versus gate bias of HfO_2 and Al_2O_3 InP MOSFETs with with 1μm gate length and V_{ds}=2V (Structure 1).

The "high-k" effect illustrate clearly in split-CV measurement of these two devices as shown in Fig. 6 where the capacitance value of HfO_2 (10nm) device is more than 60% higher than Al_2O_3 (8nm) device. That leads to 60% higher G_m for HfO_2 MOSFET, compared to Al_2O_3 MOSFET as measured in Fig.5.

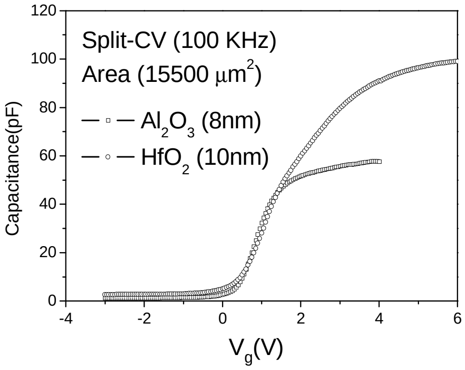


Fig.6 Split CV measurement on HfO_2 and Al_2O_3 InP MOSFETs on semi-insulating substrates.

Due to the surface channel nature of these E-mode InP MOSFETs, the drain current and G_m scales well down to 1 mm as depicted in Fig. 7. The surface channel device structure is extremely important for scalable novel devices targeting for post-CMOS application. The application of this research is for ultimate CMOS 22nm or beyond which requires the gate oxide thickness or dielectric equivalent oxide thickness (EOT) less than 1nm. To fulfill this requirement, the feasible structure is the high-k dielectrics on surface channel enhancement-mode devices.

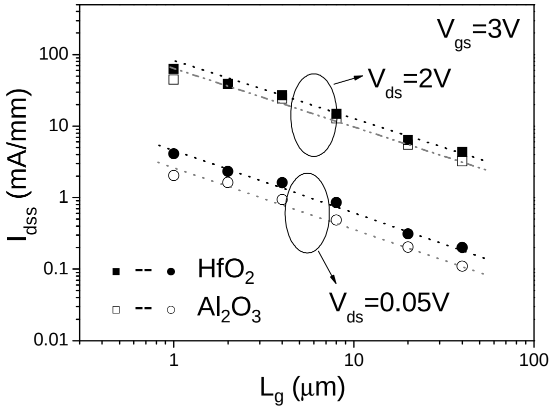


Fig.7 Drain current scalability with gate length down to 1 μm of InP MOSFETs on semi-insulating substrates.

Similar devices were also fabricated on MOCVD grown InP epi-wafers with p-type doping concentration of $1x10^{17}/cm^3$ (Structure 2) and $2x10^{17}/cm^3$. The maximum drain current drops to 17 mA/mm (Structure 3) and 20 mA/mm (Structure 2) as shown in Fig. 8. The result is consistent with what is observed in InGaAs MOSFETs.[4] The qualitative understanding of this observation is that more surface bending is required for high doping channels to realize strong inversion condition. In other words, for p-type doped InP, Fermi-level is located near the valence band maximum. If the Fermi-level and CNL is aligned at the first place, more negative charges are built in at the interface which makes further inversion more difficult.

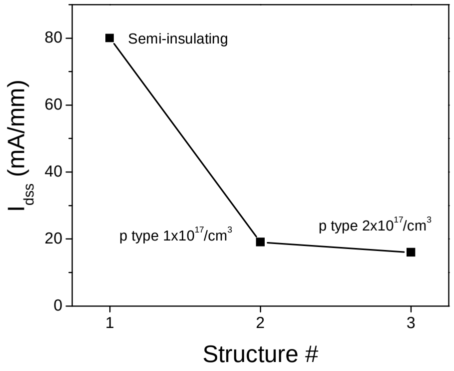


Fig.8 Comparison of maximum drain current with different InP channel doping concentration with Al_2O_3 as gate dielectric. Current in Structure 2 and Structure 3 is lower than that in Structure 1.

IV. CONCLUSION

We demonstrate here the use of ALD high-k dielectrics for the fabrication of E-mode InP MOSFETs exhibiting well-behaved transistor characteristics. These results suggest new opportunities for evaluating and applying InP as a novel high-mobility channel material for future ultimate CMOS applications.

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REFERENCES

[1] H. Becke, R. Hall, and J. White, “Gallium arsenide MOS transistors”, Solid-State Electronics, vol. **8**, no.10, pp. 813-823, Oct. 1965.

[2] T. Ito and Y. Sakai, “GaAs inversion-type MIS transistors,” Solid-State Electronics, vol. 17, no. 7, pp. 751-759, Jul. 1974.

[3] T. Mimura, K. Odani, N. Yokoyama, Y. Nakayama, and M. Fukuta, “GaAs microwave MOSFETs,” IEEE Trans. Electron Devices, vol. 25, no. 6, pp. 573-579, Jun. 1978.

[4] G.G. Fountain, R.A. Rudder, S.V. Hattangady, R.J. Markunas, and J.A. Hutchby, “Demonstration of an n-channel inversion mode GaAs MISFET”, in *IEDM Tech, Dig.,* Dec. 1989, pp. 887-889.

[5] F. Ren, M. Hong, W.S. Hobson, J.M. Kuo, J.R. Lothian, J.P. Mannaerts, J. Kwo, S.N.G. Chu, Y.K. Chen, and A.Y. Cho, “Demonstration of enhancement-mode p- and n-channel GaAs MOSFETs with $Ga_2O_3(Gd_2O_3)$ as gate oxide”, *Solid-State Electron*., vol. 41, pp. 1751-1753, 1997.

[6] F. Ren, J.M. Kuo, M. Hong, W.S. Hobson, J.R. Lothian, J. Lin, H.S. Tsai, J.P. Mannaerts, J. Kwo, S.N.G. Chu, Y.K. Chen, and A.Y. Cho, “$Ga_2O_3(Gd_2O_3)$/InGaAs enhancement-mode n-channel MOSFETs”, *IEEE Electron Devices Lett*., vol. 19, pp. 309-311, 1998.

[7] Y.C. Wang, M. Hong, J.M. Kuo, J.P. Mannaerts, J. Kwo, H.S. Tsai, J.J. Krajewski, J.S. Weiner, Y.K. Chen, and A.Y. Cho, “Advances in GaAs MOSFETs using $Ga_2O_3(Gd_2O_3)$ as gate oxide,” in Proc. Mater. Res. Soc. Symp., 1999, vol. 573, pp. 219-225.

[8] Y. Xuan, H.C. Lin, P.D. Ye, and G.D. Wilk, “Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect-transistor using atomic-layer-deposited Al_2O_3 gate dielectric”, *Appl. Phys. Lett.* vol. 88, pp. 263518-263520, 2006.

[9] K. Rajagopalan, J. Abrokwah, R. Droopad, and M. Passlack, “Enhancement-mode GaAs n-channel MOSFET”, *IEEE Electron Devices Lett*., vol. 27, pp. 959-962, Dec. 2006.

[10] I. Ok, H. Kim, M. Zhang, T. Lee, F. Zhu, L. Yu, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J.C. Lee, “Self-Aligned n- and p-channel GaAs MOSFETs on Undoped and P-type Substrates Using HfO_2 and Silicon Interface Passivation Layer”, in *IEDM Tech, Dig.,* Dec. 2006, pp. 829-832.

[11] K. Rajagopalan, R. Droopad, J. Abrokwah, P. Zurcher, P. Fejes, and M. Passlack, “1-μm Enhancement Mode GaAs N-Channel MOSFETs With Transconductance Exceeding 250 mS/mm”, *IEEE Electron Devices Lett.*, vol. 28, pp. 100-102, 2007.

[12] Y. Sun, E.W. Kiewra, S.J. Koester, N. Ruiz, A. Callegari, K.E. Fogel, D.K. Sadana, J. Fompeyrine, D.J. Webb, J.-P. Locquet, M. Sousa, and R. Germann, K.T. Shiu, and S.R. Forrest “Enhancement-mode buried-channel $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MOSFETs with high-k gate dielectrics”, *IEEE Electron Devices Lett*., vol. 28, pp. 473-475, June 2007.

[13] Y. Xuan, Y.Q. Wu, H.C. Lin, T. Shen, and P.D. Ye, “Submicrometer inversion-type enhancement-mode InGaAs MOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric”, *IEEE Electron Devices Lett*., vol. 28, pp. 935-938, Nov. 2007.

[14] Y. Xuan, Y.Q. Wu, T. Shen, T. Yang, and P.D. Ye, “High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2, HfAlO as gate dielectrics”, in *IEDM Tech, Dig.,* Dec. 2007, pp. 637-640.

[15] H.C. Lin, T. Yang, H. Sharifi, S.K. Kim, Y. Xuan, T. Shen, S. Mohammadi, and P.D. Ye, “Enhancement-mode GaAs metal-oxide-semiconductor high-electron-mobility transistors with atomic layer deposited Al_2O_3 as gate dielectric”, Applied Physics Letters, vol. 91, pp. 212101-212103, 2007.

[16] Y. Xuan, P.D. Ye, and T. Shen, “Substrate engineering for high-performance surface-channel III-V metal-oxide-semiconductor field-effect transistors”, Applied Physics Letters, vol. 91, pp. 232107-232109, 2007.

[17] T. Yang, Y. Xuan, D. Zemlyanov, T. Shen, Y.Q. Wu, J.M. Woodall, P.D. Ye, F.S. Aguirre-Tostado, M. Milojevic, S. McDonnell, and R.M. Wallace, “Interface studies of GaAs metal-oxide-semiconductor structures using atomic-layer-deposited HfO_2/Al_2O_3 nanolaminate gate dielectric”, Applied Physics Letters, vol. 91, pp. 142122-142124, 2007.

[18] Y. Xuan, H.C. Lin, and P.D. Ye, “Simplified surface preparation for GaAs passivation using atomic layer deposited high-k dielectrics”, IEEE Trans. on Electron Devices, vol. 54, no. 8, pp. 1811-1817, Aug. 2007.

[19] P.D. Ye, G.D. Wilk, J. Kwo, B. Yang, H.-J.L. Gossmann, M. Frei, S.N.G. Chu, J.P. Mannaerts, M. Sergent, M. Hong, K. Ng, J. Bude, ““GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition”, *IEEE Electron Device Letters*, vol.24, No.4, pp. 209-211, 2003.

[20] P.D. Ye, G.D. Wilk, B. Yang, J. Kwo, H.-J.L. Gossmann, S.N.G. Chu, S. Nakahara, H.-J.L. Gossmann, J.P. Mannaerts, M. Sergent, M. Hong, K. Ng, J. Bude, “GaAs MOSFET with nm-thin dielectric grown by atomic layer deposition”, *Appl. Phys. Lett.* vol 83, pp. 180-182, 2003.

[21] P.D. Ye, G.D. Wilk, B. Yang, J. Kwo, H.-J.L. Gossmann, M. Hong, K. Ng, J. Bude, “Depletion-mode InGaAs MOSFET with oxide gate dielectric grown by atomic layer deposition”, *Appl. Phys. Lett.*, vol. 84, pp. 434-436, 2004.

[22] M.V. Fischetti and S.E. Laux, *IEEE Trans. Electron Devices* **38**, 650 (1991).

[23] Y.Q. Wu, Y. Xuan, T. Shen, P.D. Ye, Z. Cheng and A. Lochtefeld, Appl. Phys. Lett. 91, 022108 (2007).

[24] Y.Q. Wu, Y. Xuan, P.D. Ye, Z. Cheng and A. Lochtefeld, in Proceeding of 64th IEEE Device Research Conference, 117 (2007).