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Beyond Vanilla CMOS: are III/V Compounds Coming into the Mainstream?

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AmberWave Systems is a company with a pretty unusual business model. As president Richard Faubert describes it, the company mines—the word “trolls” also comes to mind—university thesis projects for interesting semiconductor technology ideas. They look for projects that showed promise in the lab but have not been pursued commercially. When AmberWave finds something it thinks has potential, it licenses the technology, brings it to the state of what Faubert calls “a compelling demonstration” and then attempts to relicense the now closer-to-commercial technology to industry.

Their first serious attempt at this turned out OK—AmberWave picked up interesting research on the behavior of MOSFET carrier mobility when the channel was placed under mechanical stress, did some initial development, and licensed the idea to, among others, Intel. That put them in on the ground floor of the whole strained-silicon movement, which has become mandatory at 90 nm and below.

So what are they doing these days? Something equally interesting. There are many good reasons to be interested in III/V materials—GaAs, for instance. They make wonderful transistors, particularly for operation at or beyond 10 GHz. They also make wonderful interfaces between the electrical and optical domains: for example in fabrication of photodetectors, photovoltaic cells—potentially three to four times more efficient than Silicon cells, but far more expensive—and light sources. But they are expensive, fussy, and generally miserable enough to work with that only a few sources provide GaAs devices, and these are expensive.

That could all change if there were a way to fabricate epitaxial III/V films on cheap Silicon wafers. Unfortunately, the epitaxial part is a challenge. The pitch of the crystal lattices in most useful III/V structures is different from that of Silicon wafers. So when you deposit a III/V film on Silicon, you end up with defects in the film, which become recombination sites and mess up the electrical characteristics you wanted in the first place.

Enter AmberWave's new idea. Based on work done at MIT, AmberWave is pursuing an approach that puts a narrow trench under the location where the designer wishes to place a spot of III/V epitaxial film.

During epitaxy, you fill in the trench first, building your way up to the surface. Then the magic: the defects, for reasons of interest mainly to solid state physicists, migrate to the bottom of the trench and, if the trench is shaped correctly, get trapped there, leaving a defect-free film on the surface.

The smaller the area of the film, the better this works, apparently. AmberWave has demonstrated film deposition with very low defect rates, and it is now researching construction of three types of devices: a photovoltaic cell for solar power applications, a resonant-tunneling diode that could be used to construct a dense two-transistor memory cell, and a planar CMOS transistor with a III/V channel.

Any one of these could turn out to be commercially interesting. There are issues, of course. To date, mixing these elements into a standard Silicon process has proved problematic for process integration reasons. No doubt it's a ways away, but the thought of having defect-free III/V films for high-mobility transistors and electro-optical devices in the arsenal of a production Silicon CMOS process could be pretty interesting in a number of ways.