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Defect reduction for lattice mismatched epitaxy via aspect ratio trapping

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Germanium and III-V materials have emerged as possible successors to Si for high-performance digital logic transistors in VLSI applications. There is significant potential for enhanced performance of both p- and n-channel FETs utilizing channel materials with large lattice mismatches with respect to the Si. Along with a large lattice mismatch, however, comes the problem of large threading dislocation densities (TDDs), which adversely impact device yield. A newly developed hetero-epitaxial method for putting large lattice mismatch (=4%) materials on silicon that mitigates the formation of TDDs—aspect ratio trapping or ART—is described.

Research into the integration of Ge and III-V compound semiconductors on Si wafers has been pursued for decades. Generally, this has been driven by one of two goals: either to add new functionality to the Si CMOS logic platform (such as the ability to generate and manipulate light signals), or to make more affordable the III-V films used in existing applications by eliminating the need for expensive III-V substrates. More recently, as Ge and III-V materials have emerged as possible successors to Si for high-performance digital logic transistors in VLSI applications, a third motivation has emerged. Great performance potential, as measured by digital switching figures of merit, has been shown in n-channel field effect transistors (FETs) with InGaAs, InAs, and InSb channels [1-3]—materials with up to a 19% lattice mismatch with silicon.

Meanwhile, Ge has been widely pursued as the optimal material for ultra-high mobility PMOS devices [4,5]. Given the numerous economic and material advantages of silicon substrates, and the massive manufacturing infrastructure that has been built up around their use, a Ge and III-V on Si solution is essential if such potential is to be realized. In this paper we will discuss, in the context of previous approaches, a newly developed hetero-epitaxial method for putting large lattice-mismatch (>4%) materials on silicon, which we refer to as aspect ratio trapping (ART).

The hetero-epitaxial approach

For large lattice-mismatch, the key to any hetero-epitaxial approach is to somehow manage the dense network of crystal dislocation loops that form during the process of plastic relaxation unless the films are kept impractically thin.

Taking as an example GaAs or Ge on Si (both 4% mismatch), the so-called “critical thickness” for plastic relaxation is ˜2nm. If this thickness is significantly exceeded, many horizontal “misfit” dislocation segments will form in the plane of the epi/substrate interface to relieve the strain. If these segments are long enough, they can terminate at the wafer edge. Unfortunately, most misfits terminate in threading dislocation segments that rise up to the epi surface. For III-V or Ge films grown directly on Si, the threading dislocation density (TDD) at the epi surface is typically well above $10^8/cm^2$.

While it is certainly possible to fabricate and demonstrate research FET devices on such material, and even to show good mobility and transconductance performance, it is highly unlikely that such TDD levels could be acceptable for a yielding, reliable VLSI product. Although the correlation between TDD and VLSI yield is not well understood, based on experience with threading dislocations in early SOI material, it has been predicted that TDD likely needs to be $10^5/cm^2$ or lower to maintain negligible microprocessor yield loss [6].

Reducing TDD in hetero-epitaxial films

Much research into reducing TDD in hetero-epitaxial films can be broadly grouped into two categories. In the compositional grading approach, the lattice constant is slowly increased during epi growth. By allowing each low-mismatch layer to plastically relax before increasing the lattice constant, low TDD can be maintained throughout the epi process. Although thick buffers (˜10μm for 4% mismatch) are required for this approach to be effective, TDD well below $10^6/cm^2$ can be maintained. Grading with SiGe [7,8], for example, Ge on Si of sufficient quality to serve as a platform for GaAs lasers [9] has been demonstrated.

Alternately, the high TDD levels that arise from direct growth of high-mismatch films on silicon can be reduced via defect annihilation, occurring when two dislocations with the proper orientation meet. This process can be enhanced through various means, such as high-temperature anneals [10,11], or inclusion of strained layers [12,13]. The limit of approaches relying on annihilation is unclear, but it appears unlikely that TDD of $10^6/cm^2$ or below is practically obtainable.

In contrast to these approaches, ART invokes a third mechanism: trapping threading dislocations segments—specifically, between vertical dielectric sidewalls that confine selective growth regions, as first demonstrated in [14]. We have shown that dislocations for Ge and GaAs on Si can be largely eliminated with just a few hundred nm of epi growth, and without any high-temperature anneals [15,16]. For these reasons, the ART approach should be especially compatible with the thermal budget limits and planarity requirements of Si VLSI processing.

Defect trapping

Figure 1a shows a cross-section transmission electron micrograph (XTEM) of Ge grown on (100) silicon via the ART method (using standard low-pressure chemical vapor deposition [LPCVD]) in trenches of 200nm width etched through a SiO_2 masking layer [15]. Defect trapping is achieved within 200nm of the Si surface. For trenches up to 400nm in width, we have observed effective trapping as long as the trench aspect ratio (depth/width) is >1.

Detailed TEM studies reveal that facets, when formed early during growth, influence the orientation of dislocation segments, in effect guiding them to the trench sidewalls as the epi growth proceeds [17]. This relation between the dislocations and the faceting is key to the effectiveness of the trapping process.

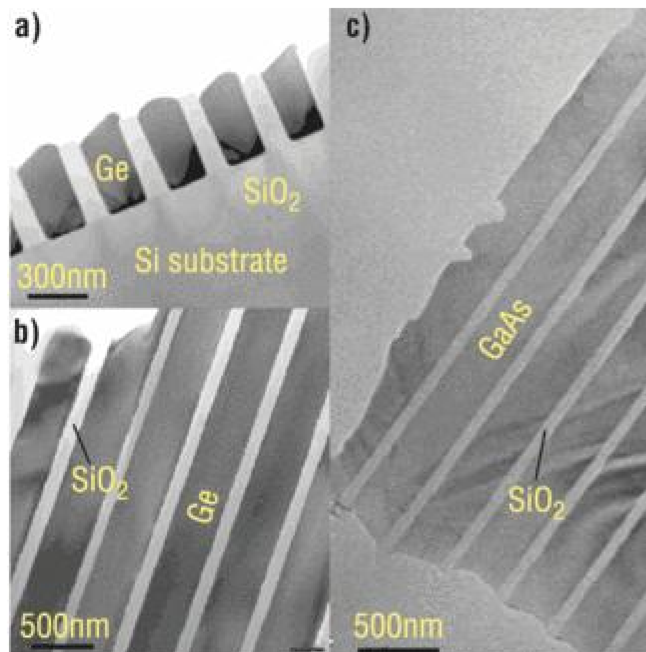

Figure 1. *TEM of Ge and GaAs grown on Si substrates via the ART method.* ***a)*** *XTEM of Ge/Si;* ***b)*** *PVTEM of Ge/Si; the upper left portion of the sample has been inadvertently removed during preparation for TEM;* ***c)*** *PVTEM of GaAs/Si; dark/light striations in GaAs regions, as well as rough edge of film, are artifacts of TEM sample preparation. SOURCE for a) and b): [15] (Copyright AIP 2007).*

While cross-section TEM is useful for understanding dislocation behavior, it is not suitable for quantifying dislocation density unless it is well above $1\times10^8/cm^2$. Plan-view TEM images include more of the sample's top surface, enabling a somewhat finer TDD estimate. **Figure 1b** shows a plan-view TEM (PVTEM) of ART growth of Ge on Si in trenches with a width >300nm [15]. The silicon substrate and the portion of the Ge film nearest the substrate (where the defect trapping occurs) have been removed as part of the sample preparation. What remains is free of defects; however, due to the small sample size, this merely sets an upper limit for TDD in the low $10^7/cm^2$ regime. TDD could be far lower than this; there appears to be nothing fundamental barring full dislocation trapping by this technique.

Quantifying true TDD

Improved metrology methods are being explored to quantify the true TDD achieved via ART, and will be reported on in the near future. **Figure 1c** shows PVTEM for the ART technique applied to GaAs grown via metal organic CVD (MOCVD) directly on (100) Si [16]. Similar to the Ge results, the top portion of the epi appears to be free of dislocations.

We have developed planarization processes to remove the faceted surface that results on top of ART epi regions, to achieve Ge and GaAs islands with flat surfaces that are co-planar with the surrounding oxide [18]. Such islands, dielectrically isolated from each other in a manner very similar to shallow trench isolation (STI)-isolated silicon active areas in a modern CMOS process, should be well suited to serve as the active areas for individual transistors. The ART region trench widths achieved to date (400nm for Ge/Si, and 300nm for GaAs/Si) should be more than sufficient for modern active area dimensions. Also, because it is selective and requires minimal epi growth, ART is ideal for putting regions of different materials (with different lattice constants) on the same wafer, which may be necessary to achieve optimal solutions for both *n*- and *p*-channel FETs. Finally, because thick, continuous epi films are avoided, thermal stress problems associated with mismatched coefficients of thermal expansion are also greatly reduced.

Conclusion

We have demonstrated a method for selectively integrating regions of large-mismatch semiconductors on silicon wafers, requiring only minimal epi growth, which should be well suited to serve as non-Si FET active areas. Key areas for further advancement of the ART technique include extending it to larger mismatch materials, as well as to larger areas suitable for a wider range of device applications.

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References

1. S. Datta et al., "85nm Gate Length Enhancement and Depletion Mode InSb Quantum-Well Transistors for Ultra-High Speed and Very-Low Power Digital Logic Applications," 2005 IEEE IEDM, p. 783.
2. M.K. Hudait et al., "Heterogeneous Integration of Enhancement Mode In0.7Ga0.3As Quantum-Well Transistor on Silicon Substrate using Thin (=2µm) Composite Buffer Architecture for High-Speed and Low-voltage (0.5V) Logic Applications," 2007 IEEE IEDM, p. 625.
3. D.-H. Kim et al., "Logic Performance of 40nm InAs HEMTs," 2007 IEEE IEDM, p. 629.
4. M. Lee et al., "Strained Ge Channel p-type Metal?oxide?semiconductor Field-effect Transistors Grown on Si1-xGex / Si Virtual Substrates," *Appl. Phys. Lett.* 79, 2001, p. 3344.
5. C.O. Chui et al., "A sub-400°C Germanium MOSFET Technology with High-*k* Dielectric and Metal Gate," 2002 IEEE IEDM, p. 437.
6. M.L. Alles et al., "Analysis of Thin Film SOI Material Defect Requirements for Advanced Circuit Applications," 1997 IEEE SOI Conf., p. 128.

7. E.A. Fitzgerald et al., “Relaxed GexSi1-x Structures for III-V Integration with Si and High-mobility Two-dimensional Electron Gases in Si,” *J. Vac. Sci. Tech.* B 10, 1992, p. 1807.
8. M.T. Currie et al., “Controlling Threading Dislocation Densities in Ge on Si using Graded SiGe Layers and Chemical-mechanical Polishing,” *Appl. Phys. Lett.* 72, 1998. p. 1718.
9. M.E. Groenert et al., “Monolithic Integration of Room-temperature CW GaAs/AlGaAs Lasers on Si Substrates via Relaxed Graded GeSi Buffer Layers,” *J. Appl. Phys.* 93, 2003, p. 362.
10. J.W. Lee et al., “Defect Reduction by Thermal Annealing of GaAs Layers Grown by Molecular Beam Epitaxy on Si Substrates,” *Appl. Phys. Lett.* 50, 1987, p. 31.
11. M. Yamaguchi et al., “Thermal Annealing Effects of Defect Reduction in GaAs on Si Substrates,” *J. Appl. Phys.* 68, 1990, p. 4518.
12. N.A. El-Masry el al., “Interactions of Dislocations in GaAs Grown on Si Substrates with InGaAs-GaAsP Strained Layered Superlattices,” *J. Appl. Phys.* 64, 1998, p. 3672.
13. Y. Takano et al., “Reduction of Threading Dislocations by InGaAs Interlayer in GaAs Layers Grown on Si Substrates,” *Appl. Phys. Lett.* 73, 1998, p. 2917.
14. T.A. Langdo et al., “High Quality Ge on Si by Epitaxial Necking,” *Appl. Phys. Lett.* 76, 2000, p. 3700.
15. J.-S. Park et al., “Defect reduction of selective Ge epitaxy in trenches on Si, 001?substrates using aspect ratio trapping,” *Appl. Phys. Lett.* 90, 052113 (2007).
16. J.Z. Li et al., “Defect Reduction of GaAs Epitaxy on Si 001?using Selective Aspect Ratio Trapping,” *Appl. Phys. Lett.* 91, 021114 (2007).
17. J. Bai et al., “Study of the Defect Elimination Mechanisms in Aspect Ratio Trapping Ge Growth,” *Appl. Phys. Lett.* 90, 101902 (2007).
18. J. Park et al, “Aspect Ratio Trapping, a New Approach to Heteroepitaxy of Ge and III-Vs on Si,” presented at ISTDM 2008 (Hsinchu, Taiwan).

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